Intel® Stratix® 10 Device Schematic Review Worksheet

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# Introduction

This document is intended to help you review your schematic and compare the pin usage against the [Intel® Stratix® 10 Device Family Pin Connection Guidelines (PDF)](https://www.intel.com/content/www/us/en/docs/programmable/683028/current/device-family-pin-connection-guidelines.html), and other referenced literature for this device family. The technical content is divided into focus areas such as, FPGA power supplies, transceiver power supplies and pin usage, configuration, FPGA I/O, and external memory interfaces.

Within each focus area, there is a table that contains the voltage or pin name for all the dedicated and dual-purpose pins of this device family. The device density and package combination may not include some of the pins shown in this worksheet, in which case, cross reference with the pin-out file for your specific device. Links to the device pin-out files are provided at the top of each section.

Before using this worksheet to review your schematic and commit to a board layout, Intel highly recommends:

1. Reviewing the latest version of the [Errata Sheet for Intel Stratix 10 Devices (PDF)](https://www.intel.com/content/www/us/en/docs/programmable/683376/current/gx-device-errata.html), and the Knowledge Database for [Intel Stratix 10 Device Known Issues](https://www.intel.com/content/www/us/en/support/programmable/kdb-filter.html#sort=%40articlepublisheddate%20descending).
2. Compiling your design in the Intel® Quartus® Prime Software to completion.

For example, there are many I/O related placement restrictions and VCCIO requirements for the I/O standards used in this device. If a complete project is not available, a top-level project should be used, with all I/O pins defined and placed, and by applying all of the configurable options that you plan to use. The project should comprise all I/O related IP, including, but not limited to, external memory interfaces, transceiver IPs, PLLs, and source synchronous SerDes. Use the I/O Analysis tool in the Intel Quartus Prime Pin Planner to validate the pinout in the Intel Quartus Prime Software to ensure that there are no conflicts with the device rules and guidelines.

When using the I/O Analysis tool you must ensure that there are no errors with the pin-out. You should also check all warning and critical warning messages to evaluate their impact on your design. Right click any of the warning or critical warning messages, and select “**Help**”. This opens a new Help window with further information on the cause of the warning, and the action that is required.

For example, the following warning is generated when a PLL is driven by a global network, where the source is a valid dedicated clock input pin, but the pin is not one dedicated to the particular PLL:

**Warning:** PLL "<PLL Instance Name>" input clock inclk[0] is not fully compensated and may have reduced jitter performance because it is fed by a non-dedicated input.

Info: Input port INCLK[0] of node "<PLL Instance Name>" is driven by clock~clkctrl which is OUTCLK output port of Clock Control Block type node clock~clkctrl

The Help file provides the following information:

**CAUSE:** The specified PLL's input clock is not driven by a dedicated input pin. As a result, the input clock delay will not be fully compensated by the PLL. Additionally, jitter performance depends on the switching rate of other design elements. This can also occur if a global signal assignment is applied to the clock input pin, which forces the clock to use the non-dedicated global clock network.

**ACTION:** If you want compensation for the specified input clock or better jitter performance, connect the input clock only to an input pin, or assign the input pin only to a dedicated input clock location for the PLL. If you do not want compensation for the specified input clock, then set the PLL to No Compensation mode.

When assigning the input pin to the proper dedicated clock pin location, refer to the [Intel Stratix 10 Clocking and PLL User Guide (PDF)](https://www.intel.com/content/www/us/en/docs/programmable/683195/20-3/clocking-and-pll-overview.html) for the proper port mapping of the dedicated clock input pins to PLLs.

Many reports are available for use after a successful compilation or an I/O analysis. For example, use the “All Package Pins” and “I/O Bank Usage” reports within the Compilation – Fitter – Resource Section to see all the I/O standards and I/O configurable options that are assigned to the pins in your design, as well as view the required VCCIO for each I/O bank. These reports must match your schematic pin connections.

The review table has the following headings:

|  |  |  |  |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |

* Plane/Signal lists the FPGA voltage or signal pin name. Edit this column to remove dedicated or dual-purpose pin names that are not available for your device density and package option.
* Schematic Name is to enter your schematic names for the signals or the plane connected to the FPGA pins.
* Connection Guidelines should be considered “read only” as they contain Intel’s recommended connection guidelines for the voltage plane or signal.
* Comments/Issues are provided as a “notepad” to comment on any deviations from the connection guidelines, and to verify that the guidelines are met. In many cases, there are notes that provide further information and details that complement the connection guidelines.

An example of how the worksheet can be used:

|  |  |  |  |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| <Plane / Signal name provided by Intel>  VCC | <user entered text>  +0.85 V | <Device Specific Guidelines provided by Intel> | <user entered text>  Connected to +0.85 V plane, no isolation is necessary.  Missing low and medium range decoupling, check PDN.  See Notes (1-1) (1-2). |

# Core Pins

## Reference Documents

Table 2‑1. Reference Documents

|  |
| --- |
| Document |
| [Documentation: Intel Stratix 10 Devices](https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/docs.html) |
| [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/support/programmable/support-resources/devices/lit-dp.html#stratix-10) |
| [Intel Stratix 10 Device Family Pin Connection Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683028/current/device-family-pin-connection-guidelines.html) |
| [Power Analyzer Support Resources](https://www.intel.com/content/www/us/en/support/programmable/support-resources/power/pow-powerplay.html) |
| [Board Developer Center](https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-guidance/board-developer.html) |
| [Intel Stratix 10 Configuration User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683762/22-1/configuration-user-guide.html) |
| [Intel Stratix 10 JTAG Boundary-Scan Testing User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683762/22-1/configuration-user-guide.html) |
| [USB-Blaster Download Cable User Guide (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/archives/ug-usb-blstr-15.1.pdf) |
| [ByteBlaster II Download Cable User Guide (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_bbii.pdf) |
| [EthernetBlaster II Communications Cable User Guide (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ethernetblasterii.pdf) |
| [AN 583: Designing Power Isolation Filters with Ferrite Beads for Altera FPGAs (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an583.pdf) |
| [AN 597: Getting Started Flow for Board Designs (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an597.pdf) |
| [AN 692: Power Sequencing Considerations for Intel Arria 10 and Intel Stratix 10 Devices](https://www.intel.com/content/www/us/en/docs/programmable/683725/current/overview-and-related-information.html#nik1412640086729) |
| [AN 778: Intel Stratix 10 L-Tile/H-Tile Transceiver Usage (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an778.pdf) |
| [Known Intel Stratix 10 Issues](https://www.intel.com/content/www/us/en/support/programmable/kdb-filter.html) |

Table 2‑2. Clock and PLL Pins

| Clock and PLL Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| CLK\_[2] [A,B,C,F,G,H,I,J,K,L,M,N]\_[0,1]p  CLK\_[3] [A,B,C,D,E,F,G,H,I,J,K,L]\_[0,1]p |  | Dedicated high speed clock input pins that can be used for data inputs or outputs. Differential input OCT Rd, single-ended input OCT Rt, and single-ended output OCT Rs are supported on these pins.  When you do not use these pins as dedicated clock pins, you can use them as regular I/O pins.  Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime Software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND. | Verify Guidelines have been met or list required actions for compliance. |
| CLK\_[2] [A,B,C,F,G,H,I,J,K,L,M ,N]U[1,2]\_[0,1]p  CLK\_[3] [A,B,C,D,E,F,G,H,I,J,K ,L]U[1,2]\_[0,1]p  [Intel Stratix 10 GX 10M Device] |  |
| CLK\_[2] [A,B,C,F,G,H,I,J,K,L,M,N]\_[0,1]n  CLK\_[3] [A,B,C,D,E,F,G,H,I,J,K,L]\_[0,1]n |  |
| CLK\_[2] [A,B,C,F,G,H,I,J,K,L,M ,N]U[1,2]\_[0,1]n  CLK\_[3] [A,B,C,D,E,F,G,H,I,J,K ,L]U[1,2]\_[0,1]n  [Intel Stratix 10 GX 10M Device] |  |
| PLL\_[2]  [A,B,C,F,G,H,I,J,K,L,M,N]\_FB[0]  PLL\_[3]  [A,B,C,F,G,H,I,J,K,L]\_FB[0] |  | Dual-purpose I/O pins that can be used as single-ended inputs, single-ended outputs, or external feedback input pins.  For more information about the supported pins, refer to the [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/programmable/support/literature/lit-dp.html).  Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime Software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND. | Verify Guidelines have been met or list required actions for compliance. |
| PLL\_[2] [A,B,C,F,G,H,I,J,K ,L, M,N]U[1,2]\_FB[0,1]  PLL\_[3] [A,B,C,D,E,F,G,H,I,J, K,L]\_ U[1,2]\_FB[0,1]  [Intel Stratix 10 GX 10M Device] |  |
| PLL\_[2] [A,B,C,F,G,H,I,J,K,L,M,N]\_FBp  PLL\_[3] [A,B,C,F,G,H,I,J,K,L]\_FBp |  | Dual-purpose I/O pins that can be used as differential I/Os, or external feedback input pins.  For more information about the supported pins, refer to the [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/programmable/support/literature/lit-dp.html).  Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime Software programmable options to internally bias these pins. | Verify Guidelines have been met or list required actions for compliance. |
| PLL\_[2] [A,B,C,F,G,H,I,J,K,L,M,N]\_FBn  PLL\_[3] [A,B,C,F,G,H,I,J,K,L]\_FBn |  |
| PLL\_[2]  [A,B,C,F,G,H,I,J,K,L,M,N]\_CLKOUT[0:1]  PLL\_[3]  [A,B,C,F,G,H,I,J,K,L]\_CLKOUT[0:1]  PLL\_[2] [A,B,C,F,G,H,I,J,K,L,M,N]\_CLKOUT[0:1]p  PLL\_[3]  [A,B,C,F,G,H,I,J,K,L]\_CLKOUT[0:1]p |  | I/O pins that can be used as two single-ended clock output pins or as one differential clock output pair.  For more information about the supported pins, refer to the [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/programmable/support/literature/lit-dp.html).  Tie the unused pins to GND or leave them unconnected. If the pins are not connected, use the Intel Quartus Prime Software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND. | Verify Guidelines have been met or list required actions for compliance. |
| PLL\_[2] [A,B,C,F, G,H,I,J,K,L,M ,N]U[ 1,2]\_CLKO UT[0:1]  PLL\_[3] [A,B,C,D, E,F,G,H,I,J,K ,L]\_ U[1,2]\_CL KOUT[0:1]  PLL\_[2] [A,B,C,F, G,H,I,J,K,L,M ,N]U[ 1,2]\_CLKO UT[0:1]p  PLL\_[2] [A,B,C,D, E,F,G,H,I,J,K ,L]U[ 1,2]\_CLKO UT[0:1]p  [Intel Stratix 10 GX 10M Device] |  |
| PLL\_[2][A,B,C,F,G,H,I,J,K,L,M,N]\_CLKOUT[0:1]n  PLL\_[3][A,B,C,F,G,H,I,J,K,L]\_CLKOUT[0:1]n  PLL\_[2] [A,B,C,F, G,H,I,J,K,L,M ,N]U[ 1,2]\_CLKO UT[0:1]n  PLL\_[3] [A,B,C,D, E,F,G,H,I,J,K ,L]U[ 1,2]\_CLKO UT[0:1]n  [Intel Stratix 10 GX 10M Device] |  |

Table 2‑3. Dedicated Configuration/JTAG Pins

| Dedicated Configuration/JTAG Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| nCONFIG |  | The nCONFIG pin is used to clear the device and prepare for reconfiguration.  When you use the Avalon-ST configuration scheme, connect this pin to the configuration host.  When you use other configuration schemes, pull this pin to the VCCIO\_SDM through an external 10 KΩ pull-up resistor.  This pin can be used to restart configuration by driving it low and then high again. Ensure that you follow all the requirements for the nCONFIG operation as specified in the [Intel Stratix 10 Configuration User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683762/22-1/configuration-user-guide.html) and [Intel Stratix 10 Device Design Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683738/current/device-design-guidelines.html). | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_nCONFIG  [Intel Stratix 10 GX 10M Device] |  |
| nSTATUS |  | This pin is used for synchronization with the configuration host driving nCONFIG, and to report errors.  **Attention**: Ensure that during power up, no external component drives the nSTATUS signal low.  When you are using the Avalon-ST configuration scheme, connect this pin to the configuration host.  For other configuration schemes, you can use this pin to monitor the configuration status.  This pin must be pulled up through a 10 kΩ resistor to VCCIO\_SDM for all configuration schemes. This pin has an internal 25 kΩ pull-up. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_nSTATUS  [Intel Stratix 10 GX 10M Device] |  |
| OSC\_CLK\_1 |  | This pin is used as the clock for device configuration and transceiver calibration.  You must provide an external clock source to this pin if you are using transceivers. If you choose to use the external clock source for  configuration and/or instantiate any transceivers in your design, you must provide a 25 MHz, 100 MHz, or 125 MHz free-running clock source to this pin and enable it in the Intel Quartus Prime Software when you compile your design. If you are using the internal oscillator for configuration and do not instantiate any transceivers in your design, leave this pin unconnected. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_OS C\_CLK\_1  [Intel Stratix 10 GX 10M Device] |  |
| TCK |  | Dedicated JTAG test clock input pin. This pin can also be used to access the SDM and HPS JTAG chains.  Connect this pin through a 1 kΩ pull-down resistor to GND.  This pin has an internal 25 kΩ pull-down.  Do not drive voltage higher than the VCCIO\_SDM supply for the TCK pin. The TCK input pin is powered by the VCCIO\_SDM supply. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_TC K  [Intel Stratix 10 GX 10M Device] |  |
| TMS |  | Dedicated JTAG test mode selects input pin. This pin can also be used to access the SDM and HPS JTAG chains.  Connect this pin to a 1 kΩ – 10 kΩ pull-up resistor to the VCCIO\_SDM supply. If the JTAG interface is not used, connect the TMS pin to the VCCIO\_SDM supply using a 1 kΩ resistor.  This pin has an internal 25 kΩ pull-up.  Do not drive voltage higher than the VCCIO\_SDM supply for the TMS pin. The TMS input pin is powered by the VCCIO\_SDM supply. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_TM S  [Intel Stratix 10 GX 10M Device] |  |
| TDI |  | Dedicated JTAG test data input pin. This pin can also be used to access the SDM and HPS JTAG chains.  Connect this pin to a 1 kΩ – 10 kΩ pull-up resistor to the VCCIO\_SDM supply. If the JTAG interface is not used, connect the TDI pin to the VCCIO\_SDM supply using a 1 kΩ resistor.  This pin has an internal 25 kΩ pull-up.  Do not drive voltage higher than the VCCIO\_SDM supply for the TDI pin. The TDI input pin is powered by the VCCIO\_SDM supply. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_TD I  [Intel Stratix 10 GX 10M Device] |  |
| TDO |  | Dedicated JTAG test data output pin. This pin can also be used to access the SDM and HPS JTAG chains.  If the JTAG interface is not used, leave the TDO pin unconnected. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_TD O  [Intel Stratix 10 GX 10M Device] |  |

Table 2‑4. Optional/Dual-Purpose Configuration Pins

| Optional/Dual-Purpose Configuration Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| AVST\_DATA[31:0] |  | Dual-purpose configuration data input pins.  Use DATA [15:0] pins for Avalon Streaming Interface (Avalon-ST) x16 mode, DATA [31:0] pins for Avalon-ST x32 mode, or as regular I/O pins.  Avalon-ST x8 mode uses the SDM\_IO pins.    These pins can also be used as user I/O pins after configuration.  If these pins are not used as the dual-purpose pins and they are not used as I/O pins, leave these pins unconnected. | Verify Guidelines have been met or list required actions for compliance. |
| AVST\_CLK |  | Dual-purpose Avalon-ST interface clock input pin.  This pin is used for Avalon-ST x16 and x32 configuration schemes.  This pin can also be used as a user I/O pin after configuration.  Connect this pin to the clock signal of an external configuration controller when configuring using the Avalon-ST x16 or x32 interface. | Verify Guidelines have been met or list required actions for compliance. |
| AVST\_VALID |  | Dual-purpose Avalon-ST interface data valid input pin.  This pin is used for Avalon-ST x16 and x32 configuration schemes.  This pin can also be used as a user I/O pin after configuration.  Connect this pin to the data valid signal of an external configuration controller when configuring using the Avalon-ST x16 or x32 interface. | Verify Guidelines have been met or list required actions for compliance. |
| nPERST[L,R][0:2] |  | Dual-purpose fundamental reset pin that is only available when you use together with PCI Express hard IP (HIP).  When the PCIe HIP on a side (left or right) is enabled, the nPERST pins on that side cannot be used as general-purpose I/Os (GPIOs). In this case, connect the nPERST pin to the system PCIe nPERST signal to ensure that both ends of the link start link-training at the same time. The nPERST pins on a side are available as GPIOs only when the PCIe HIP on that side is not enabled.  When the pin is low, the transceivers are in reset. When the pin is high, the transceivers are out of reset. When you do not use this pin as the fundamental reset, you can use this pin as a user I/O pin.  Connect this pin as defined in the Intel Quartus Prime Software. This pin is powered by the VCCIO3V supply.  When VCCIO3V is connected to a 3.0 V supply, you must use a diode to clamp the 3.3 V LVTTL PCIe input signal to the VCCIO3V power of the device.  When VCCIO3V is connected to any voltage other than 3.0 V, you must use a level translator to shift down the voltage from 3.3 V LVTTL to the corresponding voltage level powering the VCCIO3V pin.  Only one nPERST pin is used per PCIe HIP. The Intel Stratix 10 components may have all six pins listed even when the specific component might only have 1 or 2 PCIe HIPs.  nPERSTL0 = Bottom Left PCIe HIP & CvP nPERSTL1 = Middle Left PCIe HIP (When available)  nPERSTL2 = Top Left PCIe HIP (When available)  nPERSTR0 = Bottom Right PCIe HIP (When available)  nPERSTR1 = Middle Right PCIe HIP (When available)  nPERSTR2 = Top Right PCIe HIP (When available)  For maximum compatibility, always use the bottom left PCIe HIP first, as this is the only location that supports Configuration via Protocol (CvP) using the PCIe link. | Verify Guidelines have been met or list required actions for compliance. |

Table 2‑5. 3 V Compatible I/O Pins

| 3 V Compatible I/O Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| IO3V[0,1,2,3,4,5,6,7]\_[10,12,20,22] |  | These are the 3.0 V I/O pins. Each H- or L- transceiver tile supports eight 3.0 V I/O pins. These pins support 1.2 V, 1.25 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, and 3.0 V I/O standards.  For details about the supported I/O standards, refer to the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  Connect these pins according to the I/O interface standard you are using. You must provide power to the VCCR\_GXB, VCCT\_GXB and VCCH\_GXB pins of a transceiver tile to enable the 3.0 V I/O pins within that tile. For any transceiver tiles that have their VCCR\_GXB, VCCT\_GXB and VCCH\_GXB unpowered, the corresponding 3.0 V I/O pins within that tile are disabled.  Using 3 V I/O pins from an unpowered tile can potentially result in configuration failures.  Connect unused pins as defined in the Intel Quartus Prime Software. | Verify Guidelines have been met or list required actions for compliance. |
| T[1,2,3,4 ]\_IO3V[0, 1,2,3,4,5 ,6,7]  [Intel Stratix 10 GX 10M Device] |  |

Table 2‑6. 3.3 V I/O Pins

| 3.3 V I/O Pins | | | |
| --- | --- | --- | --- |
| 1. The Intel Stratix 10 GX 400 and Intel Stratix 10 SX 400 devices in the HF35 package support 3.3 V I/Os that are not available in other devices in this package. This must be taken into consideration if you plan to migrate between devices in this package. | | | |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| IO33\_[5:0]\_[7:0] |  | These are 3.3 V I/O pins. The I/O bank is known as the 3.3 V I/O bank, and it is only available in the HF35 package of the GX400(1SG040) and SX400(1SX040) devices. These pins support 3.0 V and 3.3 V I/O.  The index of [5:0] represents the grouping of the I/O pins and the index of [7:0] represents the pin numbering within the same group. The I/O pin can be configured as an input or output within the same grouping index. When any one of the pins within the same group is configured as an input or output, the remaining pins will be configured to the same I/O direction. The same I/O buffer setting such as the slew rate and weak pull-up functions will be applied for pins within the same grouping. Intel recommends you plan the I/O resources before implementing your design.  For more details about the supported I/O standards and features, refer to the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683518/21-2/i-o-overview.html).  For more details about the I/O electrical specification, refer to the [Intel Stratix Device Datasheet 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  Connect these pins according to the I/O interface standard used in your design. To enable the 3.3 V I/O bank, you must provide 3.0 V or 3.3 V power to VCCIO3C and 1.8 V power to VCCIO3D. For unused I/O pins, leave the pins as NC. Tie VREFB3CN0 to GND. | Verify Guidelines have been met or list required actions for compliance. |

Table 2‑7. Differential I/O Pins

| Differential I/O Pins | | | |
| --- | --- | --- | --- |
| 1. The I/O pins are tristated, with a weak pull-up during power up. | | | |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| LVDS[2][A,B,C,D,E, F,G,H,I,J,K,L,M,N]\_[1:24]p  LVDS[2][A,B,C,D,E,F,G,H,I,J,K,L,M,N]\_[1:24]n  LVDS[3][A,B,C,D,E,F,G,H,I,J,K,L,M,N]\_[1:24]p  LVDS[3][ A,B,C,D,E,F,G,H,I,J,K,L,M,N]\_[1:24]n |  | These are true LVDS receiver and transmitter channels on column I/O banks. Each I/O pair can be configured as an LVDS receiver or an LVDS transmitter. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If these pins are not used for differential signaling, these pins are available as user I/O pins.  Connect unused pins as defined in the Intel Quartus Prime Software. | Verify Guidelines have been met or list required actions for compliance. |
| LVDS[2] [A,B,C,F, G,H,I,J,K ,L,M,N]U[ 1,2]\_[1:2 4] [p,n]  LVD S[3] [A,B,C,D, E,F,G,H,I ,J,K,L]U[ 1,2]\_[1:2 4][p,n]  [Intel Stratix 10 GX 10M Device] |  |
| DIFF\_3[A,D]\_[1:24][p,n] |  | These I/O banks are only available in the HF35 package of the GX 400 (1SG040), SX 400 (1ST040), and TX 400 (1SX040) devices. These pins support 1.2 V, 1.25 V, 1.35 V, 1.5 V, and 1.8 V I/O standard. The LVDS, RSDS, and mini LVDS I/O standards are only supported in the dedicated clock pin. The LVDS SERDES and EMIF functions are not supported in these I/O banks.  Bank 3D of the GX 400 (1SG040) and SX 400 (1SX040) devices in the HF35 package has a maximum of 30 I/O pins only.  Connect unused pins as defined in the Intel Quartus Prime Software. | Verify Guidelines have been met or list required actions for compliance. |

Table 2‑8. Voltage Sensor Pins

| Voltage Sensor Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| VSIGP\_[0,1] |  | 2 pairs of analog differential inputs pins used with the voltage sensor inside the FPGA to monitor external analog voltages.  Tie these pins to GND if you do not use the voltage sensor feature. For details on the usage of these pins, refer to the [Intel Stratix 10 Analog to Digital Converter User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683612/20-4/adc-overview.html).  Do not drive VSIGP and VSIGN pins until the VCCADC power rail has reached 1.62 V to prevent damage. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_VS IGP\_[0,1]  [Intel Stratix 10 GX 10M Device] |
| VSIGN\_[0,1] |  |
| F[1,2]\_VS IGN\_[0,1]  [Intel Stratix 10 GX 10M Device] |

Table 2‑9. Temperature Sensor Pins

| Temperature Sensor Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| TEMPDIODEp[0..6] |  | These pins connect to the internal temperature sensing diodes in the FPGA core and in the transceiver tiles (bias-high input).  Connect this pin to an external temperature sensing device to allow sensing of the FPGA's temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave this pin unconnected.  For more information about the locations and channel numbers of the temperature sensors, refer to the Intel Stratix 10 Analog to Digital Converter User Guide. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_TE MPDIODE0p  T[1,3]\_TE MPDIODE1p  T[2,4]\_TE MPDIODE4p  [Intel Stratix 10 GX 10M Device] |  |
| TEMPDIODEn[0..6] |  | These pins connect to the internal temperature sensing diodes in the FPGA core and in the transceiver tiles (bias-low input).  Connect this pin to an external temperature sensing device to allow sensing of the FPGA's temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave this pin unconnected.  For more information about the locations and channel numbers of the temperature sensors, refer to the Intel Stratix 10 Analog to Digital Converter User Guide. | Verify Guidelines have been met or list required actions for compliance. |
| F[1,2]\_TE MPDIODE0n  T[1,3]\_TE MPDIODE1n  T[2,4]\_TE MPDIODE4n  [Intel Stratix 10 GX 10M Device] |  |

Table 2‑10. Reference Pins

| Reference Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| RZQ\_[2][A,B,C,F,G,H,I,J,K,L,M,N]  RZQ\_[3][A,B,C,D,E,F,G,H,I,J,K,L]] |  | Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located.  Connect the external precision resistor to the designated pin within the bank. If not required, this pin is a regular I/O pin.  When using OCT, tie these pins to GND through either a 240 Ω or 100 Ω resistor, depending on the desired OCT impedance.  For more information on the OCT schemes, refer to the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683518/21-2/i-o-overview.html).  When you do not use these pins as dedicated input for the external precision resistor or as I/O pins, leave these pins unconnected. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ\_[2] [A,B,C,F, G,H,I,J,K,L,M ,N]U[ 1,2]  RZQ\_[3] [A,B,C,D, E,F,G,H,I,J,K ,L]U[ 1,2]  [Intel Stratix 10 GX 10M Device] |

Table 2‑11. No Connect and DNU Pins

| No Connect and DNU Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| DNU |  | Do Not Use (DNU).  Do not connect to power, GND, or any other signal. These pins must be left floating. | Verify Guidelines have been met or list required actions for compliance. |
| NC |  | Do not drive signals into these pins.  When designing for device migration, you have the option to connect these pins to either power, GND, or a signal trace depending on the pin assignment of the devices selected for migration.  However, if device migration is not a concern, leave these pins floating.  The following guidelines are for the HF35 package of the Intel Stratix 10 GX 400 or Intel Stratix 10 SX 400 to Intel Stratix 10 GX 650 or Intel Stratix 10 SX 650 device migrations:  • You must tie the I/O pin that is incompatible for vertical migration to GND.  • There are 48 I/O pins from bank 3C and 18 I/O pins from bank 3D that will be affected. You need to compare the device pin-outs and identify the affected pins.  For more information, refer to [AN 921: Device Migration Guidelines for Intel Stratix 10 HF35 Package](https://www.intel.com/content/www/us/en/docs/programmable/683163/current/introduction.html). | Verify Guidelines have been met or list required actions for compliance. |

Table 2‑12. Power Supply Pins

| Power Supply Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| VCC |  | VCC supplies power to the core.  VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator.  For details about the recommended operating conditions, refer to the Electrical Characteristics in the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  Use the Intel Stratix 10 Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCCP and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board.  See Notes 2, 3, 4, 6, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCP |  | VCCP supplies power to the periphery.  VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator.  For details about the recommended operating conditions, refer to the Electrical Characteristics in the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  Use the Intel Stratix 10 Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCCP and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board.  See Notes 2, 3, 4, 6, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCIO([2][A,B,C,F,L,M,N], [3][A,B,C,I,J,K,L]) |  | These are the supply voltage pins for the I/O banks. Each bank can support a different voltage level.  Supported VCCIO standards include the following:  • Diff HSTL/HSTL (12,15,18)  • Diff SSTL/SSTL (12,125,135, 15, 18)  • Diff HSUL/HSUL (12)  • Diff POD 12  • LVDS/Mini\_LVDS/RSDS  • 1.2 V, 1.5 V, and 1.8 V.  These VCCIO guidelines only apply to non-HF35 packages. If you are using the HF35 package of the GX 400 (1SG040), SX 400 (1SX040), and TX 400 (1ST040) devices, refer to Table 2‑6. 3.3 V I/O Pins in this document for the VCCIO3C and VCCIO3D connection guidelines.  Connect these pins to a 1.2 V, 1.25 V, 1.35 V, 1.5 V, or 1.8 V supply, depending on the I/O standard required by the specified bank.  You have the option to power down unused I/O banks by connecting its VCCIO pin to GND.  During the power-up sequence only, a transient current whose magnitude is less than the VCCIO operating static current may be observed as the VCCIO transistors become operational. This is the expected behavior and will neither cause any functional failure nor reliability concerns to the device as long as the power-up or power-down sequence is followed.  When I/O bank 3A is used for AVST x16 or AVST x32 configuration mode, you must connect the VCCIO3A power supply to the VCCIO\_SDM power supply for proper device functionality.  For more details, refer to the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683518/21-2/i-o-overview.html).  See Notes 2, 3, 4, 8, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCIO2[A, B,C,F,G,H ,I,J,K,L, M,N ]\_F[1,2]  VCCIO3[A, B,C,D,E,F ,G,H,I,J, K,L]\_F[1, 2]  [Intel Stratix 10 GX 10M Device] |  |
| VCCIO3V |  | Power supply of the 3 V I/O bank.  Connect these pins to a 1.2 V, 1.5 V, 1.8 V, 2.5 V, or a 3.0 V supply, depending on the I/O standard required by the specified bank.  VCCIO3V must be powered on for proper device operation even if the VCCIO3V banks are unused.  VCCR\_GXB, VCCT\_GXB and VCCH\_GXB must be powered up to operate the VCCIO3V bank.  For more details, refer to the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683518/21-2/i-o-overview.html).  See Notes 2, 3, 4, 8, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCIO3V\_ T[1,2,3,4 ]  [Intel Stratix 10 GX 10M Device] |  |
| VCCPT |  | Power supply for the programmable power technology and I/O pre-drivers.  Connect VCCPT to a 1.8 V low noise switching regulator. You have the option to source the following from the same regulator as the VCCPT:  • VCCIO\_SDM and VCCIO\_HPS.  • VCCIO and VCCIO\_3V, if these rails are using the same voltage level.  • VCCBAT, if this rail is using the same voltage level and the design security key feature is not required.  • VCCH\_GXB, VCCA\_PLL, VCCPLL\_SDM, VCCPLL\_HPS, and VCCADC with proper isolation filtering.  Provide a minimum decoupling of 1 uF for the VCCPT power rail near the VCCPT pin.  A floating voltage may be observed on VCCPT during device power-up and power-down sequencing due to VCCERAM, with the magnitude of the floating voltage being lower than VCCPT. This is the expected behavior and will neither cause any functional failure nor reliability concerns to the device, provided that the power-up or power-down sequence is followed.  See Notes 2, 3, 4, 7, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCIO\_SDM |  | Configuration pins power supply.  Connect these pins to a 1.8 V power supply. When dual-purpose configuration pins are used for configuration, tie VCCIO of the bank where the dual-purpose configuration pins reside to the same regulator as VCCIO\_SDM.  When these pins require the same voltage level as VCCIO, you have the option to tie them to the same regulator as VCCIO.  Provide a minimum decoupling of 47 nF for the VCCIO\_SDM power rail near the VCCIO\_SDM pin.  See Notes 2, 3, 4, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCIO\_SDM \_F[1,2]  [Intel Stratix 10 GX 10M Device] |  |
| VCCBAT |  | Battery back-up power supply for design security volatile key register.    When using the design security volatile key, connect this pin to a non-volatile battery power source in the range of 1.2 V - 1.8 V.  When not using the volatile key, tie this pin to the 1.8 V VCCPT.  This pin must be properly powered as per the recommended voltage range as the power-on reset (POR) circuitry of the Intel Stratix 10 devices monitors the VCCBAT.  Provide a minimum decoupling of 47 nF for the VCCBAT power rail near the VCCBAT pin. | Verify Guidelines have been met or list required actions for compliance. |
| VCCBAT\_F[ 1,2]  [Intel Stratix 10 GX 10M Device] |  |
| VCCA\_PLL |  | PLL analog power.  Connect VCCA\_PLL to a 1.8 V low noise switching regulator. With proper isolation filtering, you have the option to source VCCA\_PLL from the same regulator as VCCPT.  See Notes 2, 3, 4, 7, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCA\_PLL\_ F[1,2]  [Intel Stratix 10 GX 10M Device] |  |
| VCCERAM |  | Embedded memory and digital transceiver power supply.  Connect all VCCERAM pins to a 0.9 V low noise switching power supply.  VCCPLLDIG\_SDM must be sourced from the same regulator as VCCERAM with proper isolation filtering.  For more details, refer to the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  See Notes 2, 3, 7, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCPLLDIG\_SDM |  | SDM block PLL power pins.  VCCPLLDIG\_SDM must be sourced from the same regulator as VCCERAM (0.9 V), with proper isolation filtering. | Verify Guidelines have been met or list required actions for compliance. |
| VCCPLLDIG \_SDM\_F[1, 2]  [Intel Stratix 10 GX 10M Device] |  |
| VCCPLL\_SDM |  | VCCPLL\_SDM supplies analog power to the SDM block PLL.    Connect these pins to a 1.8 V low noise power supply through a proper isolation filter.  With proper isolation filtering, you have the option to source VCCPLL\_SDM from the same regulator as VCCPT when all power rails require 1.8 V.  Decoupling for these pins depends on the design decoupling requirements of the specific board.  See Notes 2, 3, 4, and 7 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCPLL\_SD M\_F[1,2]  [Intel Stratix 10 GX 10M Device] |  |
| GND |  | Device ground pins.  Connect all GND pins to the board ground plane directly. | Verify Guidelines have been met or list required actions for compliance. |
| VREFB[[2][A,B,C,F,G,H,I,J,K,L,M,N], [3][A,B,C,D,E,F,G,H,I,J,K,L]]N0 |  | Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then use these pins as voltage-reference pins for the bank.  If VREF pins are not used, connect them to either of the VCCIOs in the bank in which the pins reside or GND.  See Notes 2, 8, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VREFB2[A, B,C,F,G,H ,I,J,K,L, M,N]N0\_F[ 1,2]  VREFB3[A, B,C,D,E,F ,G,H,I,J, K,L]N0\_F[ 1,2]  [Intel Stratix 10 GX 10M Device] |  |
| VCCLSENSE |  | Differential sense line to external regulator.  VCCLSENSE and GNDSENSE are differential remote sense pins for the VCC power. Connect your regulator’s differential remote sense lines to the respective VCCLSENSE and GNDSENSE pins. This compensates for the DC IR drop associated with the PCB and device package from the VCC power. Route these connections as differential pair traces and keep them isolated from any other noise source.  You must connect the VCCLSENSE and GNDSENSE lines to the regulator’s remote sense inputs. | Verify Guidelines have been met or list required actions for compliance. |
| VCCLSENSE \_F[1,2]  [Intel Stratix 10 GX 10M Device] |  |
| GNDSENSE |  | Verify Guidelines have been met or list required actions for compliance. |
| GNDSENSE\_ F[1,2]  [Intel Stratix 10 GX 10M Device] |  |
| VCCADC |  | ADC power pin for the voltage sensors.  You must supply a low noise 1.8 V power supply to this pin if you are using the internal voltage sensors of the Intel Stratix 10 device.  When you are using the voltage sensors, tie this pin to VCCA\_PLL with proper isolation filtering.  If you are not using the voltage sensors, tie this pin to VCCA\_PLL. | Verify Guidelines have been met or list required actions for compliance. |
| VCCADC\_F[ 1,2]  [Intel Stratix 10 GX 10M Device] |  |
| VCCFUSEWR\_SDM |  | The required power supply to program (write) the optional, one-time programmable eFuses. These eFuses are an integral part of the Intel Stratix 10 security architecture. For more information, refer to the [Intel Stratix 10 Device Security User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683642/21-4/device-security-overview-s10-fm-dm.html).    A 2.4 V power supply is required on this pin if field programming of the eFuses is required. If field-programming of the eFuses is not required, tie this pin to VCCPT or leave it unconnected (floating). Do not tie this pin to GND.  If field-programming of the eFuses is required, Intel recommends you use an adjustable regulator that is set to a 2.4 V output when programming the eFuses and a 1.8 V output at all other times.  A floating voltage may be observed on the VCCFUSEWR\_SDM power during power-up and power-down sequencing due to VCCPT and/or VCCERAM, with the total magnitude of the floating voltage being lower than VCCFUSEWR\_SDM.  During the power-up sequence only, a transient current whose magnitude is less than the VCCFUSEWR\_SDM operating transient current may be observed. The floating voltage and transient current are expected behavior and will neither cause any functional failure nor reliability concerns to the device as long as the power-up or power-down sequence is followed. | Verify Guidelines have been met or list required actions for compliance. |
| VCCFUSEWR \_SDM\_F[1, 2]  [Intel Stratix 10 GX 10M Device] |  |

Table 2‑13. SDM Pins

1. The Intel Stratix 10 GX 10M device has two independent SDMs, one for each die. The Intel Stratix 10 GX 10 M device only supports the AVSTx8 configuration scheme.

| SDM Pins | | | | |
| --- | --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | | Comments / Issues |
| RREF\_SDM |  | Reference resistor input for the PLLs of the SDM interface.  Connect a 2 kΩ¸ +/-1% resistor to GND. | | Verify Guidelines have been met or list required actions for compliance. |
| F1\_RREF \_SDM F2\_RREF \_SDM  [Intel Stratix 10 GX 10M Device] |  |
| SDM\_IO0  F[1,2]\_ SDM\_IO0  [Intel Stratix 10 GX 10M Device] |  | PWRMGT\_SCL | PMBus Power Management Clock.  This pin is used as the clock pin for the PMBus interface.  By default, the PWRMGT\_SCL function is enabled in SDM\_IO14. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM\_IO0 pin.  This pin requires a pull-up resistor to the 1.8 V VCCIO\_SDM supply. Intel recommends a pull-up value of 5.1 kΩ to 10 kΩ depending on the loading of this pin.  Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V.  Connect this pin to the PMBus clock pin of your regulator.  When a –V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT\_SCL and PWRMGT\_SDA signals to the VCC voltage regulator for the PMBus master mode, and the PWRMGT\_SCL, PWRMGT\_SDA, and PWRMGT\_ALERT signals to the external master controller for the PMBus slave mode.  When the PWRMGT\_SCL pin function of the SDM\_IO pin is set to the PMBus, it is set to open-drain. | Verify Guidelines have been met or list required actions for compliance. |
| SEU\_ERROR | The SEU\_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.  The SEU\_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Intel Quartus Prime release.  Connect this output pin to an external logic that monitors the SEU event. |
| CvP\_CONFDONE | The CvP\_CONFDONE pin indicates the device has entered user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Connect this output pin to an external logic that monitors the CvP operation. The VCCIO\_SDM power supply must meet the input voltage specification of the receiving side. |
| INIT\_DONE | The INIT\_DONE pin indicates the device has entered user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Intel Quartus Prime Software. Intel recommends you use SDM\_IO0 or SDM\_IO16 to implement the INIT\_DONE function when available as it has an internal weak pull-down for the correct function of INIT\_DONE during power up.  If SDM\_IO0 and SDM\_IO16 are unavailable, SDM\_IO5 can also be used for the INIT\_DONE function when the configuration mode is set to Avalon–ST x8 or Avalon–ST x32 (AVST x8 or AVST x32), as these modes require an external 4.7 kΩ pull-down resistor.  If SDM\_IO0, SDM\_IO5, and SDM\_IO16 are unavailable, the INIT\_DONE function can also be implemented using any unused SDM I/O pins provided that an external 4.7 kΩ pulldown resistor is provided for the INIT\_DONE signal.  This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  When the INIT\_DONE function is enabled, this pin will drive high when configuration is complete, and the device goes into user mode. |
| PWRMGT\_ALERT | PMBus Power Management Alert.  This pin is used as the ALERT function for the PMBus interface when the Intel Stratix 10 –V is the PMBus slave.  You can connect either the SDM\_IO0 or SDM\_IO12 pin as the PWRMGT\_ALERT signal, and for Avalon-ST x8 and Avalon-ST x16 configuration scheme, you can also use SDM\_IO9 pin as PWRMGT\_ALERT signal.  This pin requires a pull-up resistor to the 1.8 V VCCIO\_SDM supply. Intel recommends a pullup value of 5.1 kΩ to 10 kΩ depending on the loading of this pin.  Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V.  Connect this pin to the PMBus ALERT pin of the external master controller. When using the SmartVID feature with the Intel Stratix 10 –V device as a PMBus slave, you must connect the PWRMGT\_ALERT signal along with the PWRMGT\_SCL and PWRMGT\_SDA signals to the PMBus master device to complete the SmartVID power management interface. The PMBus master device reads the VID codes from the Intel Stratix 10 slave, and programs the voltage regulator to output the correct VID voltage.  When the PWRMGT\_ALERT pin function of the SDM\_IO pin is set to the PMBus, it is set to open-drain. |
| Direct to Factory Image | Direct to factory input pin.  When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.  Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image is the default image of the device, and only switches to factory image if required. |
| HPS\_COLD\_nRESET | This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5 ms, this pin will generate interrupts to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25 kΩ pull up on this pin.  Connect this pin through a 1–10 kΩ pull up to the VCCIO\_SDM supply. Do not connect this pin to the reset input of any connected quad serial peripheral interface (quad SPI) devices. |
| SDM\_IO1  F[1,2]\_ SDM\_IO1  [Intel Stratix 10 GX 10M Device] |  | AVSTx8\_DATA2 | Avalon-ST Interface Data 2.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data2 pin of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| AS\_DATA1 | Active Serial Data 1.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data1 pin of the EPCQ-L device when configuring from the EPCQ-L device. |
| SDM\_IO3  F[1,2]\_ SDM\_IO3  [Intel Stratix 10 GX 10M Device]\ |  | AVSTx8\_DATA3 | Avalon Stream Interface Data 3  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data3 pin of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| AS\_DATA2 | Active Serial Data 2.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data2 pin of the EPCQ-L device when configuring from the EPCQ-L device. |
| SDM\_IO4  F[1,2]\_ SDM\_IO4  [Intel Stratix 10 GX 10M Device] |  | AVSTx8\_DATA1 | Avalon Stream Interface Data 1.  This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.  Connect this pin to the data1 pin of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| AS\_DATA0 | Active Serial Data 0.  This pin is pulled high internally by a 25-kΩ resistor when the device is powered up.  Connect this pin to the data0 pin of the EPCQ-L device when configuring from the EPCQ-L device. |
| SDM\_IO5  F[1,2]\_ SDM\_IO5  [Intel Stratix 10 GX 10M Device] |  | MSEL [0] | Configuration input pins that set the configuration scheme for the FPGA device.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  This pin will function as MSEL [0] during power up and reset to determine the configuration scheme.  This pin needs to be pulled-up to VCCIO\_SDM or pulled-down to GND through a 4.7 kΩ resistor depending on your configuration scheme. After the pin completes the MSEL function, it will then function according to the configuration scheme you have selected.  For more information, refer to the [Intel Stratix 10 Configuration User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683762/22-1/configuration-user-guide.html). | Verify Guidelines have been met or list required actions for compliance. |
| CONF\_DONE | The CONF\_DONE pin indicates all configuration data has been received. By default, SDM\_IO16 is the recommended pin to implement the CONF\_DONE function. If you are using the Avalon-ST x8 configuration scheme and I2C power management feature, the PWRMGT\_SDA function can be assigned to either SDM\_IO12 or SDM\_IO16. Use SDM\_IO5 to implement the CONF\_DONE function if SDM\_IO16 is used for the PWRMGT\_SDA function.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect the CONF\_DONE pin to the external configuration controller when configuring using the Avalon-ST interface. |
| AS\_nCSO0 | Active Serial Chip Select 0.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the nCS input of the first EPCQ-L device when configuring from EPCQ-L devices. |
| INIT\_DONE | The INIT\_DONE pin indicates the device has entered user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Intel Quartus Prime Software. Intel recommends you use SDM\_IO0 or SDM\_IO16 to implement the INIT\_DONE function when available as it has an internal weak pull-down for the correct function of INIT\_DONE during power up.  If SDM\_IO0 and SDM\_IO16 are unavailable, SDM\_IO5 can also be used for the INIT\_DONE function when the configuration mode is set to Avalon–ST x8 or Avalon–ST x32 (AVST x8 or AVST x32) as these modes require an external 4.7 kΩ pull-down resistor.  If SDM\_IO0, SDM\_IO5, and SDM\_IO16 are unavailable, the INIT\_DONE function can also be implemented using any unused SDM I/O pins provided that an external 4.7 kΩ pulldown resistor is provided for the INIT\_DONE signal.  This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  When the INIT\_DONE function is enabled, this pin will drive high when configuration is complete, and the device goes into user mode. |
| SDM\_IO6  F[1,2]\_ SDM\_IO6  [Intel Stratix 10 GX 10M Device] |  | AVSTx8\_DATA4 | Avalon Stream Interface Data 4.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data4 pin of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| AS\_DATA3 | Active Serial Data 3.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data3 pin of the EPCQ-L device when configuring from the EPCQ-L device. |
| SDM\_IO7  F[1,2]\_ SDM\_IO7  [Intel Stratix 10 GX 10M Device] |  | MSEL[1] | Configuration input pins that set the configuration scheme for the FPGA device.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  This pin will function as MSEL[1] during power up and reset to determine the configuration scheme.  This pin needs to be pulled-up to VCCIO\_SDM or pulled-down to GND through a 4.7kΩ resistor depending on your configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected.  For more information, refer to the [Intel Stratix 10 Configuration User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683762/22-1/configuration-user-guide.html). | Verify Guidelines have been met or list required actions for compliance. |
| AS\_nCSO2 | Active Serial Chip Select 2.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the nCS input of the third EPCQ-L device when configuring from EPCQ-L devices. |
| SDM\_IO8  F[1,2]\_ SDM\_IO8  [Intel Stratix 10 GX 10M Device] |  | AVST\_READY | Avalon Stream Interface Data Ready.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the ready signal output of the external configuration controller when configuring using the Avalon-ST x8, x16, or x32 interface. | Verify Guidelines have been met or list required actions for compliance. |
| AS\_nCSO3 | Active Serial Chip Select 3.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the nCS input of the fourth EPCQ-L device when configuring from EPCQ-L devices. |
| SDM\_IO9  F[1,2]\_ SDM\_IO9  [Intel Stratix 10 GX 10M Device] |  | PWRMGT\_ALERT | PMBus Power Management Alert.  This pin is used as the ALERT function for the PMBus interface when the Intel Stratix 10 –V is the PMBus slave.  You can connect either the SDM\_IO0 or SDM\_IO12 pin as the PWRMGT\_ALERT signal, and for Avalon-ST x8 and Avalon-ST x16 configuration scheme, you can also use SDM\_IO9 pin as PWRMGT\_ALERT signal.  This pin requires a pull-up resistor to the 1.8 V VCCIO\_SDM supply. Intel recommends a pullup value of 5.1 kΩ to 10 kΩ depending on the loading of this pin.  Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V.  Connect this pin to the PMBus ALERT pin of the external master controller. When using the SmartVID feature with the Intel Stratix 10 –V device as a PMBus slave, you must connect the PWRMGT\_ALERT signal along with the PWRMGT\_SCL and PWRMGT\_SDA signals to the PMBus master device to complete the SmartVID power management interface. The PMBus master device reads the VID codes from the Intel Stratix 10 slave and programs the voltage regulator to output the correct VID voltage.  When the PWRMGT\_ALERT pin function of the SDM\_IO pin is set to the PMBus, it is set to open-drain. | Verify Guidelines have been met or list required actions for compliance. |
| MSEL[2] | Configuration input pins that set the configuration scheme for the FPGA device.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  This pin will function as MSEL [2] during power up and reset to determine the configuration scheme.  This pin needs to be pulled-up to VCCIO\_SDM or pulled-down to GND through a 4.7 kΩ resistor depending on your configuration scheme. Once the pin completes the MSEL function, it functions according to the configuration scheme you have selected.  For more information, refer to the [Intel Stratix 10 Configuration User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683762/22-1/configuration-user-guide.html). |
| AS\_nCSO1 | Active Serial Chip Select 1.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the nCS input of the second EPCQ-L device when configuring from EPCQ-L devices. |
| SDM\_IO10  F[1,2]\_ SDM\_IO10  [Intel Stratix 10 GX 10M Device] |  | AVSTx8\_DATA7 | Avalon Stream Interface Data 7.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data7 pin of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| SEU\_ERROR | The SEU\_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.  The SEU\_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Intel Quartus Prime release.  Connect this output pin to an external logic that monitors the SEU event. |
| CvP\_CONFDONE | The CvP\_CONFDONE pin indicates the device has entered user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Connect this output pin to an external logic that monitors the CvP operation. The VCCIO\_SDM power supply must meet the input voltage specification of the receiving side. |
| Direct to factory Image | Direct to factory input pin.  When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.  Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required. |
| HPS\_COLD\_nRESET | This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5 ms, this pin will generate interrupts to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25 kΩ pull up on this pin.  Connect this pin through a 1–10 kΩ pull up to the VCCIO\_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices. |
| SDM\_IO11  F[1,2]\_ SDM\_IO11  [Intel Stratix 10 GX 10M Device] |  | AVSTx8\_VALID | Avalon Stream Interface Data Valid.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data valid pin of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_COLD\_nRESET | This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5ms, this pin will generate interrupts to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. After the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25 kΩ pull up on this pin.  Connect this pin through a 1–10 kΩ pull up to the VCCIO\_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices. |
| SEU\_ERROR | The SEU\_ERROR pin drives high to indicate that there  is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.  The SEU\_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Intel Quartus Prime release.  Connect this output pin to an external logic that monitors the SEU event. |
| CvP\_CONFDONE | The CvP\_CONFDONE pin indicates that the device has entered user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Connect this output pin to an external logic that monitors the CvP operation. The VCCIO\_SDM power supply must meet the input voltage specification of the receiving side. |
| Direct to factory Image | Direct to factory input pin.  When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.  Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required. |
| PWRMGT\_SDA | PMBus Power Management Serial Data.  This pin is used as the data pin for the PMBus interface.  By default, use the SDM\_IO11 pin for the PWRMGT\_SDA function. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM\_IO12 pin or SDM\_IO16 pin.  This pin requires a pull-up resistor to the 1.8 V VCCIO\_SDM supply. Intel recommends a pullup value of 5.1 kΩ to 10 kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V.  Connect this pin to the PMBus data pin of your regulator. When a –V device is used, you must enable the SmartVID connection between the devices and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT\_SCL and PWRMGT\_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT\_SCL, PWRMGT\_SDA, and PWRMGT\_ALERT signals to the external master controller for the PMBus slave mode.  When the PWRMGT\_SDA pin function of the SDM\_IO pin is set to the PMBus, it is set to open-drain. |
| SDM\_IO12  F[1,2]\_ SDM\_IO12  [Intel Stratix 10 GX 10M Device] |  | PWRMGT\_ALERT | PMBus Power Management Alert.  This pin is used as the ALERT function for the PMBus interface when the Intel Stratix 10 –V is the PMBus slave.  You can connect either the SDM\_IO0 or SDM\_IO12 pin as the PWRMGT\_ALERT signal, and for Avalon-ST x8 and Avalon-ST x16 configuration scheme, you can also use SDM\_IO9 pin as PWRMGT\_ALERT signal.  This pin requires a pull-up resistor to the 1.8 V VCCIO\_SDM supply. Intel recommends a pullup value of 5.1 kΩ to 10 kΩ depending on the loading of this pin.  Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V.  Connect this pin to the PMBus ALERT pin of the external master controller. When using the SmartVID feature with the Intel Stratix 10 –V device as a PMBus slave, you must connect the PWRMGT\_ALERT signal along with the PWRMGT\_SCL and PWRMGT\_SDA signals to the PMBus master device to complete the SmartVID power management interface. The PMBus master device reads the VID codes from the Intel Stratix 10 slave and programs the voltage regulator to output the correct VID voltage.  When the PWRMGT\_ALERT pin function of the SDM\_IO pin is set to the PMBus, it is set to open-drain. | Verify Guidelines have been met or list required actions for compliance. |
| SEU\_ERROR | The SEU\_ERROR pin drives high to indicate that there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.  The SEU\_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Intel Quartus Prime release.  Connect this output pin to an external logic that monitors the SEU event. |
| CvP\_CONFDONE | The CvP\_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Connect this output pin to an external logic that monitors the CvP operation. The VCCIO\_SDM power supply must meet the input voltage specification of the receiving side. |
| Direct to factory Image | Direct to factory input pin.  When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.  Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required. |
| PWRMGT\_SDA | PMBus Power Management Serial Data.  This pin is used as the data pin for the PMBus interface.  By default, use the SDM\_IO11 pin for the PWRMGT\_SDA function. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM\_IO12 pin or SDM\_IO16 pin.  This pin requires a pull-up resistor to the 1.8 V VCCIO\_SDM supply. Intel recommends a pullup value of 5.1 kΩ to 10 kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V.  Connect this pin to the PMBus data pin of your regulator. When a –V device is used, you must enable the SmartVID connection between the devices and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT\_SCL and PWRMGT\_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT\_SCL, PWRMGT\_SDA, and PWRMGT\_ALERT signals to the external master controller for the PMBus slave mode.  When the PWRMGT\_SDA pin function of the SDM\_IO pin is set to the PMBus, it is set to open-drain. |
| HPS\_COLD\_nRESET | This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5 ms, this pin will generate interrupts to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25 kΩ pull up on this pin.  Connect this pin through a 1–10 kΩ pull up to the VCCIO\_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices. |
| SDM\_IO13  F[1,2]\_ SDM\_IO13  [Intel Stratix 10 GX 10M Device] |  | AVSTx8\_DATA5 | Avalon Stream Interface Data 5.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data5 pin of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| SEU\_ERROR | The SEU\_ERROR pin drives high to indicate that there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.  The SEU\_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Intel Quartus Prime release.  Connect this output pin to an external logic that monitors the SEU event. |
| CvP\_CONFDONE | The CvP\_CONFDONE pin indicates that the device has entered user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Connect this output pin to an external logic that monitors the CvP operation. The VCCIO\_SDM power supply must meet the input voltage specification of the receiving side. |
| Direct to factory Image | Direct to factory input pin.  When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.  Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required. |
| HPS\_COLD\_nRESET | This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5 ms, this pin will generate interrupts to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25 kΩ pull up on this pin.  Connect this pin through a 1–10 kΩ pull up to the VCCIO\_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices. |
| SDM\_IO14  F[1,2]\_ SDM\_IO14  [Intel Stratix 10 GX 10M Device] |  | AVSTx8\_CLK | Avalon Stream Interface Clock Input.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the clock output of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_COLD\_nRESET | This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5 ms, this pin will generate interrupts to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25 kΩ pull up on this pin.  Connect this pin through a 1–10 kΩ pull up to the VCCIO\_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices. |
| SEU\_ERROR | The SEU\_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.  The SEU\_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Intel Quartus Prime release.  Connect this output pin to an external logic that monitors the SEU event. |
| CvP\_CONFDONE | The CvP\_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Connect this output pin to an external logic that monitors the CvP operation. The VCCIO\_SDM power supply must meet the input voltage specification of the receiving side. |
| Direct to factory Image | Direct to factory input pin.  When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.  Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required. |
| PWRMGT\_SCL | PMBus Power Management Clock.  This pin is used as the clock pin for the PMBus interface.  By default, the PWRMGT\_SCL function is enabled in SDM\_IO14. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM\_IO0 pin.  This pin requires a pull-up resistor to the 1.8 V VCCIO\_SDM supply. Intel recommends a pullup value of 5.1 kΩ to 10 kΩ depending on the loading of this pin.  Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V.  Connect this pin to the PMBus clock pin of your regulator.  When a –V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT\_SCL and PWRMGT\_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT\_SCL, PWRMGT\_SDA, and PWRMGT\_ALERT signals to the external master controller for the PMBus slave mode.  When the PWRMGT\_SCL pin function of the SDM\_IO pin is set to the PMBus, it is set to open-drain. |
| SDM\_IO15  F[1,2]\_ SDM\_IO15  [Intel Stratix 10 GX 10M Device] |  | AVSTx8\_DATA6 | Avalon Stream Interface Data 6.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect this pin to the data6 pin of an external configuration controller when configuring using the Avalon-ST x8 interface. | Verify Guidelines have been met or list required actions for compliance. |
| SEU\_ERROR | The SEU\_ERROR pin drives high to indicate that there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.  The SEU\_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Intel Quartus Prime release.  Connect this output pin to an external logic that monitors the SEU event. |
| CvP\_CONFDONE | The CvP\_CONFDONE pin indicates that the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Connect this output pin to an external logic that monitors the CvP operation. The VCCIO\_SDM power supply must meet the input voltage specification of the receiving side. |
| Direct to factory Image | Direct to factory input pin.  When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.  Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required. |
| HPS\_COLD\_nRESET | This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5 ms, this pin will generate interrupts to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. After the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25 kΩ pull up on this pin.  Connect this pin through a 1–10 kΩ pull up to the VCCIO\_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices. |
| SDM\_IO16  F[1,2]\_ SDM\_IO16  [Intel Stratix 10 GX 10M Device]f |  | CONF\_DONE | The CONF\_DONE pin indicates device configuration has completed. SDM\_IO16 is the recommended pin to implement the CONF\_DONE function if this pin is enabled in the Quartus Prime software.  Intel recommends that you use this pin as it has a weak pull-down for the correct function during power up. If you are using the Avalon-ST x8 configuration scheme and I2C power management feature, the PWRMGT\_SDA function can be assigned to either SDM\_IO12 or SDM\_IO16. Use SDM\_IO5 to implement the CONF\_DONE function if SDM\_IO16 is used for the PWRMGT\_SDA function.    The CONF\_DONE function can also be implemented using the other unused SDM I/O pins.  This pin is pulled high internally by a 25 kΩ resistor when the device is powered up.  Connect the CONF\_DONE pin to the external configuration controller when configuring using the Avalon-ST interface. | Verify Guidelines have been met or list required actions for compliance. |
| PWRMGT\_SDA | PMBus Power Management Serial Data.  This pin is used as the data pin for the PMBus interface.  By default, use the SDM\_IO11 pin for the PWRMGT\_SDA function. If you use Avalon-ST x8 configuration scheme, you must implement this function using the SDM\_IO12 pin or SDM\_IO16 pin.  This pin requires a pull-up resistor to the 1.8 V VCCIO\_SDM supply. Intel recommends a pull-up value of 5.1 kΩ to 10 kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V.  Connect this pin to the PMBus data pin of your regulator. When a –V device is used, you must enable the SmartVID connection between the devices and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT\_SCL and PWRMGT\_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT\_SCL, PWRMGT\_SDA, and PWRMGT\_ALERT signals to the external master controller for the PMBus slave mode.  When the PWRMGT\_SDA pin function of the SDM\_IO pin is set to the PMBus, it is set to open-drain. |
| INIT\_DONE | The INIT\_DONE pin indicates that the device has enter user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Intel Quartus Prime Software. Intel recommends that you use SDM\_IO0 or SDM\_IO16 to implement the INIT\_DONE function when available as it has an internal weak pull-down for the correct function of INIT\_DONE during power up.  If SDM\_IO0 and SDM\_IO16 are unavailable, SDM\_IO5 can also be used for the INIT\_DONE function when the configuration mode is set to Avalon–ST x8 or Avalon–ST x32 (AVST x8 or AVST x32) as these modes require an external 4.7 kΩ pull-down resistor.  If SDM\_IO0, SDM\_IO5, and SDM\_IO16 are unavailable, the INIT\_DONE function can also be implemented using any unused SDM I/O pins provided that an external 4.7 kΩ pulldown resistor is provided for the INIT\_DONE signal.  This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  When the INIT\_DONE function is enabled, this pin will drive high when configuration is complete, and the device goes into user mode. |
| SEU\_ERROR | The SEU\_ERROR pin drives high to indicate that there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages.  The SEU\_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Intel Quartus Prime release.  Connect this output pin to an external logic that monitors the SEU event. |
| CvP\_CONFDONE | The CvP\_CONFDONE pin indicates the device has enter user mode upon completion of the CvP core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime Software. This pin is pulled low internally by a 25 kΩ resistor when the device is powered up.  Connect this output pin to an external logic that monitors the CvP operation. The VCCIO\_SDM power supply must meet the input voltage specification of the receiving side. |
| Direct to factory Image | Direct to factory input pin.  When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.  Connect this input pin to an external logic that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required. |
| HPS\_COLD\_nRESET | This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally for at least 5 ms, this pin will generate interrupts to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input. There is an internal 25 kΩ pull up on this pin.  Connect this pin through a 1–10 kΩ pull up to the VCCIO\_SDM supply. Do not connect this pin to the reset input of any connected quad SPI devices. |

### Notes on Core Pins

1. Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime Software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, packaging, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Stratix 10 GX device variant.
2. Select the capacitance values for the power supply after considering the amount of power needed to supply over the frequency of operation of the circuit being decoupled. Calculate the target impedance for the power plane based on the current draw and voltage drop requirements of the device/supply. Decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to the “Equivalent Series Inductance” of the mounting of the packages. Consider proper board design techniques, such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Stratix 10 Early Power Estimator (EPE) to determine the preliminary current requirements for the VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Stratix 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
6. Example 1 and Example 2 in the Intel Stratix 10 Device Family Pin Connection Guidelines illustrate the power supply sharing guidelines for the Intel Stratix 10 GX devices.
7. The Low Noise Switching Regulator is a switching regulator circuit encapsulated in a thin surface mount package, containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz, and has a fast transient response. The switching frequency range is not an Intel requirement.
8. The number of modular I/O banks on Intel Stratix 10 devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683518/21-2/i-o-overview.html).
9. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. Decoupling for these pins depends on the design decoupling requirements of the specific board.
11. There are no dedicated PR\_REQUEST, PR\_ERROR, and PR\_DONE pins. If required, you can use the user I/O pins for these functions.
12. The device orientation is a die view (bottom of chip view).

# High Bandwidth Memory Pins

Table 3‑1. Reference Documents

|  |
| --- |
| Document |
| [Documentation: Intel Stratix 10 Devices](https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/docs.html) |
| [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/support/programmable/support-resources/devices/lit-dp.html#stratix-10) |
| [Intel Stratix 10 Device Family Pin Connection Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683028/current/device-family-pin-connection-guidelines.html) |
| [Board Developer Center](https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-guidance/board-developer.html) |
| [AN 597: Getting Started Flow for Board Designs (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an597.pdf) |
| [Known Intel Stratix 10 Issues](https://www.intel.com/content/www/us/en/support/programmable/kdb-filter.html) |

Table 3‑2. UIB and eSRAM Pins

| UIB and eSRAM Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| CLK\_ESRAM\_[0,1]p |  | Dedicated positive high speed differential reference clock pin for eSRAM PLL.  Connect this pin to the positive terminal of an LVDS clock source within the range of 10 MHz to 325 MHz. The frequency selected must match the available options provided in the Intel Quartus Prime ESRAM PLL Reference Clock Frequency selection dialog box. Only DC-coupling is supported. The peak-to-peak jitter of this clock must meet or exceed the following jitter requirements for frequency bandwidth from 10 kHz to 1/2 of the frequency chosen:   * 20 ps peak-to-peak * 1.42 ps RMS at 1e-12 BER * 1.22 ps at 1e-16 BER   Connect directly to GND if unused.  The input reference clock must be stable and free-running at device power-up for proper PLL calibration and successful configuration. | Verify Guidelines have been met or list required actions for compliance. |
| CLK\_ESRAM\_[0,1]n |  | Dedicated complement high speed differential reference clock pin for eSRAM PLL.  Connect this pin to the negative terminal of an LVDS clock source within the range of 10 MHz to 325 MHz. The frequency selected must match the available options provided in the Intel Quartus Prime ESRAM PLL Reference Clock Frequency selection dialog box. Only DC-coupling is supported. The peak-to-peak jitter of this clock must meet or exceed the following jitter requirements for frequency bandwidth from 10 kHz to 1/2 of the frequency chosen:   * 20 ps peak-to-peak * 1.42 ps RMS at 1e-12 BER * 1.22 ps at 1e-16 BER   Connect directly to GND if unused.  The input reference clock must be stable and free-running at device power-up for proper PLL calibration and successful configuration. | Verify Guidelines have been met or list required actions for compliance. |
| CLK\_ESRAM\_[0,1]n  UIB\_PLL\_REF\_CLK\_[00,01]p |  | Dedicated positive high speed differential reference clock pin for UIB PLL.  Connect this pin to the positive terminal of an LVDS clock source within the range of 10 MHz to 325 MHz. The frequency selected must match the available options provided in the Intel Quartus Prime HBM2 interface PLL Reference Clock Frequency selection dialog box. Only DC-coupling is supported. The peak-to-peak jitter of this clock must meet or exceed the following jitter requirements for frequency bandwidth from 10 kHz to 1/2 of the frequency chosen:   * 20 ps peak-to-peak * 1.42 ps RMS at 1e-12 BER * 1.22 ps at 1e-16 BER   Provide a stable reference clock to this pin before device configuration begins when the high-bandwidth memory (HBM2) IP is included in your design.  Connect directly to GND if unused.  The input reference clock must be stable and free-running at device power-up for proper PLL calibrations and a successful configuration. | Verify Guidelines have been met or list required actions for compliance. |
| UIB\_PLL\_REF\_CLK\_[00,01]n |  | Dedicated complement high speed differential reference clock pin for UIB PLL.  Connect this pin to the negative terminal of an LVDS clock source within the range of 10 MHz to 325 MHz. The frequency selected must match the available options provided in the Intel Quartus Prime HBM2 interface PLL Reference Clock Frequency selection dialog box. Only DC-coupling is supported. The peak-to-peak jitter of this clock must meet or exceed the following jitter requirements for frequency bandwidth from 10 kHz to 1/2 of the frequency chosen:   * 20 ps peak-to-peak * 1.42 ps RMS at 1e-12 BER * 1.22 ps at 1e-16 BER   Provide a stable reference clock to this pin before device configuration begins when the high-bandwidth memory (HBM2) IP is included in your design.  Connect directly to GND if unused.  The input reference clock must be stable and free-running at device power-up for proper PLL calibrations and a successful configuration. | Verify Guidelines have been met or list required actions for compliance. |
| RREF\_ESRAM\_[0,1] |  | Reference resistor pin for UIB PLL and eSRAM PLL, specific to the top(T) and bottom(B) of the device.  If any UIB PLL or eSRAM PLL on the top or bottom side of the device is used, the corresponding RREF pin on that side (top or bottom) must connect to its own individual 2 kΩ +/-1% resistor to GND. The PCB trace between this pin and the reference resistor needs to be carefully routed to avoid any aggressor signals. | Verify Guidelines have been met or list required actions for compliance. |
| UIB\_RREF\_[00,01] |  | Reference resistor pin for UIB IO ZQ calibration.  Connect each pin through an individual 240 Ω +/-1% resistor to GND. No resistor sharing between pins is allowed. Leave this pin floating if unused. | Verify Guidelines have been met or list required actions for compliance. |

Table 3‑3. HBM Power Supply Pins

|  |  |  |  |
| --- | --- | --- | --- |
| HBM Power Supply Pins | | | |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| VCCM\_WORD\_[BL,TL] |  | Power supply for the embedded HBM2 memory.  Connect these power pins to a 2.5 V power supply. | Verify Guidelines have been met or list required actions for compliance. |
| VCCIO\_UIB\_[BL,TL] |  | Power supply for the Universal Interface Bus between the core and embedded HBM2 memory.  Connect these power pins to a 1.2 V power supply. | Verify Guidelines have been met or list required actions for compliance. |

### Notes on High Bandwidth Memory Pins

1. Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime Software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, packaging, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Stratix 10 MX device variant.
2. Select the capacitance values for the power supply after considering the amount of power needed to supply over the frequency of operation of the circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage drop requirements of the device/supply. Decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to the “Equivalent Series Inductance” of the mounting of the packages. Consider proper board design techniques, such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Stratix 10 Early Power Estimator (EPE) to determine the preliminary current requirements for the VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Stratix 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
6. Example 7 and Example 8 in the Intel Stratix 10 Device Family Pin Connection Guidelines illustrate the power supply sharing guidelines for the Intel Stratix 10 MX devices.
7. The Low Noise Switching Regulator is a switching regulator circuit encapsulated in a thin surface mount package, containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz, and has fast transient response. The switching frequency range is not an Intel requirement.
8. The number of modular I/O banks on Intel Stratix 10 devices depends on the device density. For the indexes available for a specific device, refer to the I/O Bank section in the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683518/21-2/i-o-overview.html).
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. Decoupling for these pins depends on the design decoupling requirements of the specific board.

# H-Tile/L-Tile Pins

Table 4‑1. Reference Documents

|  |
| --- |
| Document |
| [Intel Stratix 10 Recommended Reference Literature](https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/docs.html) |
| [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/support/programmable/support-resources/devices/lit-dp.html#stratix-10) |
| [Intel Stratix 10 Device Family Pin Connection Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683028/current/device-family-pin-connection-guidelines.html) |
| [Board Developer Center](https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-guidance/board-developer.html) |
| [AN 597: Getting Started Flow for Board Designs (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an597.pdf) |
| [Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683621/current/overview.html) |
| [Known Intel Stratix 10 Issues](https://www.intel.com/content/www/us/en/support/programmable/kdb-filter.html) |

Table 4‑2. H-Tile/L-Tile Pins

| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| --- | --- | --- | --- |
| VCCH\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  VCCH\_GXBL 1\_T[1,3] VCCH\_GXBR 1\_T[2,4]  [Intel Stratix 10 GX 10M Device |  | Analog power, block level transmitter buffers, specific to the left (L) side or right (R) side of the device.  Connect VCCH\_GXB to a 1.8 V low noise switching regulator. With proper isolation filtering, you have the option to source  VCCH\_GXB from the same regulator as VCCPT.  To minimize the regulator switching noise impact on channel jitter performance, keep the switching frequency for the VCCH\_GXB regulator below 2 MHz. For OTN applications,  the switching frequency for VCCH\_GXB is recommended to be below 500 KHz.  Place a 22 nF decoupling capacitor between each VCCH\_GXB power pin and GND pin on the back side of the BGA pin field.  A voltage leakage may be observed on the VCCH\_GXB power rail before the VCCH\_GXB is powered on due to leakage inside the device during the power-up and power-down sequencing. The total magnitude of this leakage voltage is lower than the VCCH\_GXB and is expected behavior.  During the power-up sequence only, a transient current whose magnitude is less than the VCCH\_GXB static operating current may be observed. Floating voltage and transient current are expected behavior and will neither cause any functional failure nor reliability concerns to the device as long as the power-up or power-down sequence is followed.  When all the transceivers on the same tile are not used, you may power down the transceivers in that tile by connecting its VCCR\_GXB, VCCT\_GXB, and VCCH\_GXB to GND.  See Notes 2, 3, 4, 7, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCT\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  VCCT\_GXBL 1[C,D,E]\_ T[1,3]  VCCT\_GXBL 1[K,L,M]\_ T[2,4]  [Intel Stratix 10 GX 10M Device] |  | Analog power and transmitter, specific to each transceiver bank of the left (L) side or right (R) side of the device.  Connect VCCT\_GXB pins to a 1.03 V or 1.12 V low noise switching regulator depending on the transceiver data rate.  VCCR\_GXB and VCCT\_GXB pins of each bank within a transceiver tile (L-tile or H-tile) must have the same voltage (either 1.03 V or 1.12 V). However, VCCR\_GXB and VCCT\_GXB of different banks within the same transceiver tile can have different voltages based on the configured transceiver data rates, to further reduce power consumption of the transceiver tile. When the banks within a transceiver tile are powered at different voltages (for example, some banks are operating at 1.03 V, while other banks are operating at 1.12 V), the xN clock lines are only allowed to transverse between contiguous banks operating at the same VCCR\_GXB or VCCT\_GXB voltages. The xN clock lines are not allowed to cross boundaries of banks operating at different voltages. Any input reference clock coming into a transceiver tile can be distributed to any bank within the tile, even if the VCCR\_GXB and VCCT\_GXB operating voltages of the banks are different.  When all the transceivers on the same tile are not used, you can power down the transceivers in that tile by connecting its VCCR\_GXB, VCCT\_GXB, and VCCH\_GXB to GND.  Place a 22 nF decoupling capacitor between each VCCT\_GXB power pin and GND pin on the back side of the BGA pin field.  The VCCR\_GXB and VCCT\_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device, as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  See Notes 2, 3, 4, 7, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| VCCR\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  VCCR\_GXBL 1[C,D,E]\_ T[1,3]  VCCR\_GXBL 1[K,L,M]\_ T[2,4]  [Intel Stratix 10 GX 10M Device] |  | Analog power and receiver, specific to each transceiver bank of the left (L) side or right (R) side of the device.  Connect VCCR\_GXB pins to a 1.03 V or 1.12 V low noise switching regulator depending on the transceiver data rate.  VCCR\_GXB and VCCT\_GXB pins of each bank within a transceiver tile (L-tile or H-tile) must have the same voltage (either 1.03 V or 1.12 V). However, VCCR\_GXB and VCCT\_GXB of different banks within the same transceiver tile can have different voltages based on the configured transceiver data rates, to further reduce power consumption of the transceiver tile. When the banks within a transceiver tile are powered at different voltages (for example, some banks are operating at 1.03 V while other banks are operating at 1.12 V), the xN clock lines are only allowed to transverse between contiguous banks operating at the same VCCR\_GXB or VCCT\_GXB voltages. The xN clock lines are not allowed to cross boundaries of banks operating at different voltages. Any input reference clock coming into a transceiver tile, can be distributed to any bank within the tile even if the VCCR\_GXB and VCCT\_GXB operating voltages of the banks are different.  When all the transceivers on the same tile are not used, you can power down the transceivers in that tile by connecting its VCCR\_GXB, VCCT\_GXB, and VCCH\_GXB to GND.    Place a 22 nF decoupling capacitor between each VCCR\_GXB power pin and GND pin on the back side of the BGA pin field.  The VCCR\_GXB and VCCT\_GXB voltage supplies can vary depending on whether it is an L-tile or H-tile device, as well as the channel configuration (non-bonded versus bonded channels) on each tile. For more information about the voltage requirement for your specific use case, refer to the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  See Notes 2, 3, 4, 7, and 10 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_RX\_CH[0:5]p  GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_REFCLK[0:5]p  T1\_GXBL1[ C,D,E,F]\_ RX\_CH [0:5 ]P  T1\_GXBL1[ C,D,E,F]\_ REFCLK [0: 5]p  T2\_GXBL1[ N,M,L,K]\_ RX\_CH [0:5 ]P  T2\_GXBL1[ N,M,L,K]\_ REFCLK [0: 5]p  T3\_GXBL1[ C,D,E,F]\_ RX\_CH [0:5 ]P  T3\_GXBL1[ C,D,E,F]\_ REFCLK [0: 5]p  T4\_GXBL1[ N,M,L,K]\_ RX\_CH [0:5 ]P  T4\_GXBL1[ N,M,L,K]\_ REFCLK [0: 5]p  [Intel Stratix 10 GX 10M Device] |  | High speed positive differential receiver channels or REFCLK inputs. Specific to each transceiver bank of the left (L) side or right (R) side of the device.  These pins can be AC-coupled or DC-coupled when used. For more information, refer to the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  Connect all unused GXB\_RX\_CH []p pins directly to GND. | Verify Guidelines have been met or list required actions for compliance. |
| GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_RX\_CH[0:5]n  GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_REFCLK[0:5]n  T1\_GXBL1[ C,D,E,F]\_ RX\_CH [0:5 ]n  T1\_GXBL1[ C,D,E,F]\_ REFCLK [0: 5]n  T2\_GXBL1[ N,M,L,K]\_ RX\_CH [0:5 ]n  T2\_GXBL1[ N,M,L,K]\_ REFCLK [0: 5]n  T3\_GXBL1[ C,D,E,F]\_ RX\_CH [0:5 ]n  T3\_GXBL1[ C,D,E,F]\_ REFCLK [0: 5]n  T4\_GXBL1[ N,M,L,K]\_ RX\_CH [0:5 ]n  T4\_GXBL1[ N,M,L,K]\_ REFCLK [0: 5]n  [Intel Stratix 10 GX 10M Device] |  | High speed negative differential receiver channels or REFCLK inputs. Specific to each transceiver bank of the left (L) side or right (R) side of the device.  These pins can be AC-coupled or DC-coupled when used. For more information, refer to the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  Connect all unused GXB\_RX\_CH[]n pins directly to GND. | Verify Guidelines have been met or list required actions for compliance. |
| GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_TX\_CH[0:5]p  T1\_GXBL1[ C,D,E,F]\_ TX\_CH [0:5 ]p  T2\_GXBL1[ N,M,L,K]\_ TX\_CH [0:5 ]p  T3\_GXBL1[ C,D,E,F]\_ TX\_CH [0:5 ]p  T4\_GXBL1[ N,M,L,K]\_ TX\_CH [0:5 ]p  [Intel Stratix 10 GX 10M Device] |  | High speed positive differential transmitter channels. Specific to each transceiver bank of the left (L) side or right (R) side of the device.  Leave all unused GXB\_TX\_CH[]p pins floating. | Verify Guidelines have been met or list required actions for compliance. |
| GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_TX\_CH[0:5]n  T1\_GXBL1[ C,D,E,F]\_ TX\_CH [0:5 ]n  T2\_GXBL1[ N,M,L,K]\_ TX\_CH [0:5 ]n  T3\_GXBL1[ C,D,E,F]\_ TX\_CH [0:5 ]n  T4\_GXBL1[ N,M,L,K]\_ TX\_CH [0:5 ]n  [Intel Stratix 10 GX 10M Device] |  | High speed negative differential transmitter channels. Specific to each transceiver bank of the left (L) side or right (R) side of the device.  Leave all unused GXB\_TX\_CH[]n pins floating. | Verify Guidelines have been met or list required actions for compliance. |
| REFCLK\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]p  T1\_REFCLK \_GXBL1[C, D,E,F] \_CH[B,T]p  T2\_REFCLK \_GXBL1[N, M,L,K] \_CH[B,T]p  T3\_REFCLK \_GXBL1[C, D,E,F] \_CH[B,T]p  T4\_REFCLK \_GXBL1[N, M,L,K] \_CH[B,T]p  [Intel Stratix 10 GX 10M Device] |  | High speed differential reference clock positive receiver channels, specific to each transceiver bank of the left (L) side or right (R) side of the device.  REFCLK\_GXB can be used as dedicated clock input pins with fPLL for core clock generation, even when the transceiver channel is not used.  These pins should be AC-coupled when connected to any I/O standard other than the HCSL I/O standard. For the HCSL I/O standard, these pins must be DC-coupled. For example, PCIe reference clocks should be DC-coupled if they use the HCSL I/O standard.  Connect each unused REFCLK\_GXB pin to GND plane directly on its own via. Do not share vias when connecting to GND.  The input reference clock must be stable and free-running at device power-up for proper PLL calibrations and successful configuration. For PCIe, you must follow this clock requirement.  See Note 9 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| REFCLK\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]n  T1\_REFCLK \_GXBL1[C, D,E,F] \_CH[B,T]n  T2\_REFCLK \_GXBL1[N, M,L,K] \_CH[B,T]n  T3\_REFCLK \_GXBL1[C, D,E,F] \_CH[B,T]n  T4\_REFCLK \_GXBL1[N, M,L,K] \_CH[B,T]n  [Intel Stratix 10 GX 10M Device] |  | High speed differential reference clock complement, complementary receiver channel, specific to each transceiver bank of the left (L) side or right (R) side of the device.  REFCLK\_GXB can be used as dedicated clock input pins with fPLL for core clock generation even when the transceiver channel is not used.    These pins should be AC-coupled when connected to any I/O standard other than the HCSL I/O standard. For the HCSL I/O standard, these pins must be DC-coupled. For example, PCIe reference clocks should be DC-coupled if they use the HCSL I/O standard.  Connect each unused REFCLK\_GXB pin to GND plane directly on its own via. Do not share vias when connecting to GND.  The input reference clock must be stable and free-running at device power-up for proper PLL calibrations and successful configuration. For PCIe, you must follow this clock requirement.  See Note 9 in Notes on Core Pins. | Verify Guidelines have been met or list required actions for compliance. |
| RREF\_[T,M,B][L,R]  T1\_RREF\_B L  T2\_RREF\_B R  T3\_RREF\_B L  T4\_RREF\_B R  [Intel Stratix 10 GX 10M Device] |  | Reference resistor for fPLL, IOPLL, and transceiver, specific to the top (T), middle (M), and bottom (B) of the left (L) side or right (R) side of the device.  If any REFCLK pin or transceiver channel on one side (left or right) of the device, IOPLL, or fPLL is used, you must connect each RREF pin on that side of the device to its own individual 2 kΩ +/-1% resistor to GND.  Otherwise, you can connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals. | Verify Guidelines have been met or list required actions for compliance. |
| RREF\_SIPAUX0 |  | Reference resistor pin for UIB PLL.  Connect the RREF\_SIPAUX0 pin to a 2 kΩ ±1% resistor to GND. In the PCB layout, the trace from this pin to the resistor must be routed so that it avoids any aggressor signals. | Verify Guidelines have been met or list required actions for compliance. |

# E-Tile Pins

Table 5‑1. Reference Documents

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| --- |
| Document |
| [Intel Stratix 10 Recommended Reference Literature](https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/docs.html) |
| [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/support/programmable/support-resources/devices/lit-dp.html#stratix-10) |
| [Intel Stratix 10 Device Family Pin Connection Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683028/current/device-family-pin-connection-guidelines.html) |
| [Board Developer Center](https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-guidance/board-developer.html) |
| [AN 597: Getting Started Flow for Board Designs (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an597.pdf) |
| [E-Tile Transceiver PHY User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683723/current/e-tile-transceiver-phy-overview.html) |
| Intel Stratix 10 E-Tile Channel Placement Tool |
| [Known Intel Stratix 10 Issues](https://www.intel.com/content/www/us/en/support/programmable/kdb-filter.html) |

Table 5‑2. E-Tile Pins

| E-Tile Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| VCCH\_GXE(L2, L3, R1,  R2, R3) |  | Analog power, block level transmitter buffers for E-tile, specific to the left (L) side or right (R) side of the device.  Connect VCCH\_GXE to a 1.1 V low noise switching regulator. VCCH\_GXE must be powered up even when the E-tile transceivers are not used. | Verify Guidelines have been met or list required actions for compliance. |
| VCCRT\_GXE(L2, L3, R1,  R2, R3) |  | Analog power, used for high-speed circuitry for the E-tile blocks, specific to the left (L) side or right (R) side of the device.  Connect VCCRT\_GXE to VCCERAM through an LC filter. For more information about the LC filter design, refer to the [Intel Stratix 10 Power Management User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683418/21-1/power-management-overview.html).  VCCRT\_GXE must be powered up even when the E-tile transceivers are not used. | Verify Guidelines have been met or list required actions for compliance. |
| VCCRTPLL\_GXE(L2, L3,  R1, R2, R3) |  | Analog power, used for high-speed circuitry for the E-tile blocks, specific to the left (L) side or right (R) side of the device.  Source the VCCRTPLL\_GXE from the VCCRT\_GXE with proper isolation filtering.  Filtering may be optional if this voltage rail can meet the noise mask requirement. For more information about the noise mask requirements, refer to the [Intel Stratix 10 Power Management User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683418/21-1/power-management-overview.html).  VCCRTPLL\_GXE must be powered up even when the E-tile transceivers are not used. | Verify Guidelines have been met or list required actions for compliance. |
| VCCCLK\_GXE(L2, L3, R1,  R2, R3) |  | I/O power, specific to the E-tile reference clock buffers.  Connect VCCCLK\_GXE to a 2.5 V low noise switching regulator.  VCCCLK\_GXE must be powered up even when the E-tile transceivers are not used. | Verify Guidelines have been met or list required actions for compliance. |
| GXE(L8, R9)(A, B,  C)\_RX\_CH[0:23][p,n] |  | High speed differential serial inputs to the receiver circuitry. Specific to the E-tile transceiver blocks on the left (L) side or right (R) side of the device.  For PAM4, no off-chip AC-coupling capacitor is required, provided that the RX input common mode voltage is between (GND + 300 mV) and (VCCH\_GXE-300 mV), and the RX input amplitude differential voltage is less than 1200 mVp-p. For PAM4, the absolute maximum positive voltage at the RX input of the SerDes is VCCH\_GXE to maintain linearity.  For NRZ, no off-chip AC-coupling capacitor is required provided that the RX input common mode voltage is between GND and VCCH\_GXE, and the RX input amplitude differential voltage is less than 1200 mVp-p. For NRZ, the absolute maximum positive voltage at the RX input to the SerDes is (VCCH\_GXE + 300 mV) to prevent forward-biasing of the ESD diodes.  For more information, refer to the Electrical Characteristics section in the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html).  When the RX input common mode voltage is outside its required range (PAM4 or NRZ), external AC-coupling capacitors must be used. When using external AC-coupling capacitors, the RX termination is to the VCCH\_GXE supply. A typical value of 100 nF can be used as the external AC coupling capacitor. Select a capacitor package (SMD) similar to that of the trace width, to reduce in-line parasitics, and a material of X7R quality or higher. For high speed SerDes, the mounting launch pad must be carefully designed.  For more information about external AC-coupling, refer to the [Intel Stratix 10 E-Tile Transceiver PHY User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683723/current/e-tile-transceiver-phy-overview.html).  Leave unused pins floating. | Verify Guidelines have been met or list required actions for compliance. |
| GXE(L8, R9)(A, B,  C)\_TX\_CH[0:23][p,n] |  | High speed differential serial outputs from the transmitter circuitry. Specific to the E-tile transceiver blocks on the left (L) side or right (R) side of the device.  Leave all unused GXE\_TX[p,n] pins floating. | Verify Guidelines have been met or list required actions for compliance. |
| REFCLK\_GXE(L8,R9)  (A,B,C)\_CH[0:8][p,n] |  | High speed differential reference clock. Connects to the E-tile transceiver of the left(L) side or right (R) side of the device.  REFCLK\_GXE is supplied to both RX and TX independently. REFCLK\_GXE can be used as dedicated clock input pins for core clock generation by configuring the transceiver channel (Native PHY IP core) in the PLL mode.  Supported I/O standard: LVPECL  No off-chip AC-coupling capacitor is required. The default internal REFCLK inputs are 2.5 V LVPECL with a 50 Ω termination. Optional external termination is 2.5 V LVPECL or 3.3 V LVPECL. For more information about the external termination, refer to section 4.1 in the [Intel Stratix 10 E-Tile Transceiver PHY User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683723/current/e-tile-transceiver-phy-overview.html).  Tie each unused REFCLK pin to GND through a 1 kΩ resistor.  REFCLK[1] must always be bonded out on board and connected to a clock source in case dynamic reconfiguration of REFCLK is planned. For more details on how to use it, refer to section 7.12 in the [Intel Stratix 10 E-Tile Transceiver PHY User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683723/current/e-tile-transceiver-phy-overview.html).  Preservation of unused transceiver channels may need extra REFCLK\_GXE to be bonded out on board based on use cases. For more details, refer to section 3.1.10 Unused Transceiver Channel in the [Intel Stratix 10 E-Tile Transceiver PHY User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683723/current/e-tile-transceiver-phy-overview.html).  The input reference clock must be stable and free-running at device power-up for proper PLL calibrations and a successful configuration. | Verify Guidelines have been met or list required actions for compliance. |
| IO\_AUX\_RREF(11, 12,  20, 21, 22) |  | Reference resistor for the AIB auxiliary channel.  Connect to a 2 kΩ resistor (±1%) to GND. | Verify Guidelines have been met or list required actions for compliance. |

### Notes for E-Tile Pins

1. Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime Software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, packaging, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Stratix 10 GX device variant.
2. Select the capacitance values for the power supply after considering the amount of power needed to supply over the frequency of operation of the circuit being decoupled. Calculate the target impedance for the power plane based on the current draw and voltage drop requirements of the device/supply. Decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to the “Equivalent Series Inductance” of the mounting of the packages. Consider proper board design techniques, such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Stratix 10 Early Power Estimator (EPE) to determine the preliminary current requirements for the VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Stratix 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
6. Example 9 and Example 10 in the Intel Stratix 10 Device Family Pin Connection Guidelines illustrate the power supply sharing guidelines for the Intel Stratix 10 GX devices.
7. The Low Noise Switching Regulator is a switching regulator circuit encapsulated in a thin surface mount package, containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz, and has a fast transient response. The switching frequency range is not an Intel requirement.
8. The number of modular I/O banks on Intel Stratix 10 devices depends on the device density. For the indexes available for a specific device, refer to the I/O Bank section in the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683518/21-2/i-o-overview.html).
9. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. Decoupling for these pins depends on the design decoupling requirements of the specific board.

# P-Tile Pins

Table 6‑1. Reference Documents

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| --- |
| Document |
| [Intel Stratix 10 Recommended Reference Literature](https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/docs.html) |
| [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/support/programmable/support-resources/devices/lit-dp.html#stratix-10) |
| [Intel Stratix 10 Device Family Pin Connection Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683028/current/device-family-pin-connection-guidelines.html) |
| [Board Developer Center](https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-guidance/board-developer.html) |
| [AN 597: Getting Started Flow for Board Designs (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an597.pdf) |
| [Intel FPGA P-Tile Avalon Streaming IP for PCI Express User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683059/22-1-8-0-0/about-the-p-tile-fpga-ips-for-pci-express.html) |
| [Intel FPGA P-Tile Avalon Memory-mapped IP for PCI Express User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683268/21-1-4-0-0/introduction.html) |
| [Known Intel Stratix 10 Issues](https://www.intel.com/content/www/us/en/support/programmable/kdb-filter.html) |

Table 6‑2. P-Tile Pins

| P-Tile Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| VCCH\_GXP[L, R][1, 2, 3] |  | Secondary high-voltage analog supply for transceivers and on-die PLL specific to the P-tile.  Connect VCCH\_GXP to a 1.8 V low-noise switching regulator. Place a 22 nF decoupling capacitor between each VCCH\_GXP power pin and GND pin on the back side of the BGA pin field.  VCCH\_GXP must be filtered through the ferrite bead.  VCCH\_GXP must be powered up even when the P-tile transceivers are not used. | Verify Guidelines have been met or list required actions for compliance. |
| VCCRT\_GXP[L, R][1, 2, 3] |  | Primary analog supply for the TX and RX channels, specific to the P-tile.  Connect VCCRT\_GXP to a 0.9 V low-noise switching regulator. With proper isolation filtering, you have the option to source VCCRT\_GXP from the same regulator as VCCERAM.  VCCRT\_GXP must be powered up even when the P-tile transceivers are not used. | Verify Guidelines have been met or list required actions for compliance. |
| VCCCLK\_GXP[L, R][1, 2, 3] |  | LVCMOS I/O buffer supply rail, specific to the P-tile.  Connect VCCCLK\_GXP to a 1.8 V low-noise switching regulator. With proper isolation filtering, you have the option to source VCCCLK\_GXP from the same regulator as VCCPT.  VCCCLK\_GXP must be powered up even when the P-tile transceivers are not used. | Verify Guidelines have been met or list required actions for compliance. |
| VCCFUSE\_GXP |  | Required power supply for firmware to read internal settings for the one-time programmable eFuses.  Connect the VCCFUSE\_GXP pin to the 0.9 V VCCERAM power. Connecting to the VCCERAM power rail adheres to the power down sequencing requirement for the VCCFUSE\_GXP supply. Do not leave this pin floating, or tie it to GND.  VCCFUSE\_GXP must be powered up even when the P-tile transceivers are not used. | Verify Guidelines have been met or list required actions for compliance. |
| IO\_AUX\_RREF[10, 11,  12, 20, 21, 22]\_P |  | Reference resistor for the P-tile transceivers.  Connect each IO\_AUX\_RREF pin to a 2.8 KΩ resistor (±1%) to GND.  In the PCB layout, the trace from this pin to the resistor needs to be routed such that it avoids any aggressor signals.  If this tile is unused, you must connect the 2.8 KΩ resistor between this pin and GND. | Verify Guidelines have been met or list required actions for compliance. |
| U[10, 11, 12, 20, 21,  22]\_P\_IO\_RESREF\_0 |  | Transceiver reference resistor connection for PMA circuitry to provide termination for calibration.  Connect each pin to a 169 Ω (±1%, 100 ppm/C) precision resistor to GND, if the UltraPath Interconnect (UPI)/PCIe is 85 Ω impedance.  Place this resistor very close to the IO\_RESREF pin. Avoid routing any noisy signals next to this reference resistor or its traces. Tie the resistor to GND plane through a via placed very close to the reference resistor.  The external reference resistor parasitic capacitance load must be less than 6.5 pF. | Verify Guidelines have been met or list required actions for compliance. |
| I\_PIN\_PERST\_N[10, 11,  12, 20, 21, 22]\_P |  | PCI Express (PCIe) Platform reset pin.  In a PCI Express (PCIe) adapter card implementation, connect the PCIe nPERST signal from the PCIe edge connector to each P-tile transceiver bank I\_PIN\_PERST\_N input.  Use a level translator to fan out and change the 3.3 V open-drain nPERST signal from the PCIe connector to the 1.8 V I\_PIN\_PERST\_N input of each P-tile transceiver that is used on the board.  Provide a 1.8 V pull-up resistor to the I\_PIN\_PERST\_N input, as the nPERST signal from the PCIe connector is an open-drain signal. Pull up the 3.3 V PCIe nPERST signal on the adapter card.  For the UltraPath Interconnect (UPI) mode, contact Intel for guidance.  If the tile is unused, tie it to GND. | Verify Guidelines have been met or list required actions for compliance. |
| GXP[L, R][10, 11, 12]  [A, B, C]\_TX\_CH[0:19]  [p,n] |  | Differential-based transmitter pins, specific to the P-tile transceivers on the left (L) side and right (R) side of the device.  These pins support NRZ encoding up to 16 Gbps.  Connection guidelines for the PCIe and UltraPath Interconnect (UPI) modes are as follows:   * PCIe mode—TX pins must be AC coupled. Capacitor values range from 176 nF to 256 nF per PCIe Gen 4 specification. * UPI mode—TX pins must be DC coupled.   When these pins are not used, they can be floating. | Verify Guidelines have been met or list required actions for compliance. |
| GXP[L, R][10, 11, 12]  [A, B, C]\_RX\_CH[0:19]  [p,n] |  | Differential-based receiver pins, specific to the P-tile transceivers on the left (L) side and right (R) side of the device.  These pins support NRZ encoding up to 16 Gbps.  When these pins are not used, they can be left floating. | Verify Guidelines have been met or list required actions for compliance. |
| REFCLK\_GXP[L, R][10,  11, 12][A, B, C]\_CH[0,  2][p,n] |  | Standard PCIe HCSL reference clock input pins, specific to the P-tile transceivers on the left (L) side and right (R) side of the device.  The HCSL I/O standard only supports DC-coupling. In the PCIe configuration, DC-coupling is allowed on the REFCLK if the selected REFCLK I/O standard is the HCSL I/O standard.  Connect each unused REFCLK\_GXP pin to GND plane directly on its own via. Do not share vias when connecting to GND.  Connect a 100 MHz reference clock to both reference clock inputs for x16 and 4x4 modes. These reference clocks must be derived from the same clock source. A fan-out buffer can be used but must meet a ±300 ppm requirement. For 2x8 modes, connect both reference clock inputs to the same clock source or connect to two independent clock sources.  If the P-tile is completely unused but still has power applied, tie both REFCLK inputs to GND. | Verify Guidelines have been met or list required actions for compliance. |
| S\_STRAP[10,11,12,20,21  ,22]\_P |  | Internal strap pins.  For PCIe only systems, connect to GND.  For UltraPath Interconnect (UPI) applications, connect the strap pins as follows:   * For a two socket (2S) Intel® Xeon® system, connect to GND. * For a four socket (4S) Intel Xeon system, pull up through a 10 kΩ resistor to VCCCLK\_GXP (1.8 V).   For more information on the UltraPath Interconnect (UPI) mode, contact Intel for guidance. | Verify Guidelines have been met or list required actions for compliance. |
| NODE\_ID[0,1]  [10,11,12,20,21,22]\_P |  | Internal node ID pins.  For PCIe only systems, connect both ID pins to GND.  For UltraPath Interconnect (UPI) applications, connect these ID pins to the corresponding CPU ID of the UPI interface.   * NODE\_ID0 connects to CPU0. * NODE\_ID1 connects to CPU1.   If the tile is unused, tie to GND.  For more information on the UltraPath Interconnect (UPI) mode, contact Intel for guidance. | Verify Guidelines have been met or list required actions for compliance. |

# Hard Processor System Pins

Table 7‑1. Reference Documents

|  |
| --- |
| Document |
| [Intel Stratix 10 Recommended Reference Literature](https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/docs.html) |
| [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/support/programmable/support-resources/devices/lit-dp.html#stratix-10) |
| [Intel Stratix 10 Device Family Pin Connection Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683028/current/device-family-pin-connection-guidelines.html) |
| [Board Developer Center](https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-guidance/board-developer.html) |
| [AN 597: Getting Started Flow for Board Designs (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an597.pdf) |
| [Known Intel Stratix 10 Issues](https://www.intel.com/content/www/us/en/support/programmable/kdb-filter.html) |

Table 7‑2. HPS Supply Pins

| HPS Supply Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| VCCL\_HPS |  | VCCL\_HPS supplies power to the HPS core.  The VCCL\_HPS power supply voltage could vary from 0.8 V to 0.94 V, for –1V, –2V, or –3V devices with the SmartVID feature depending on the SmartVID setting in the device. When using –2L or –3X devices, connect to either a 0.9 V or 0.94 V supply. When using 0.9 V supply, VCCL\_HPS can be connected to VCCERAM.  VCCL\_HPS can be shared with VCC and VCCP if they are at the same voltage level only when using –1V, –2V, or –3V devices (with the SmartVID feature). VCCL\_HPS cannot be shared with VCC and VCCP when using –2L or –3X devices. VCCL\_HPS always needs to be equal to VCCPLLDIG\_HPS.  Use the Intel Stratix 10 Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCCL\_HPS and other power supplies.  Decoupling for these pins depends on the design decoupling requirements of the specific board.  See Notes 2, 3, 4, and 6 in the Notes on HPS Pins.  If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave VCCL\_HPS floating or connected to GND. | Verify Guidelines have been met or list required actions for compliance. |
| VCCIO\_HPS |  | The HPS dedicated I/Os support a 1.8 V voltage level.  Connect these pins to a 1.8 V power supply. If these pins have the same voltage requirement as VCCIO and VCCIO\_SDM, you have the option to source VCCIO\_HPS pins from the same regulator as VCCIO and VCCIO\_SDM.  Decoupling for these pins depends on the design decoupling requirements of the specific board.  See Notes 2, 3, 4, and 8 in the Notes on HPS Pins.  If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave VCCIO\_HPS floating or connected to GND. | Verify Guidelines have been met or list required actions for compliance. |
| VCCPLL\_HPS |  | VCCPLL\_HPS supplies analog power to the HPS core PLLs.  Connect these pins to a 1.8 V low noise power supply, through a proper isolation filter. You have the option to share VCCPLL\_HPS with the same regulator as VCCPT when all power rails require 1.8 V, but only with a proper isolation filter.  Decoupling for these pins depends on the design decoupling requirements of the specific board.  See Notes 2, 3, 4, and 7 in the Notes on HPS Pins.  If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave VCCPLL\_HPS floating or connected to GND. | Verify Guidelines have been met or list required actions for compliance. |
| VCCPLLDIG\_HPS |  | Digital power supply of the PLL in HPS.  Connect this to the VCCL\_HPS with proper isolation filtering.  For more information about isolation filters, refer to [AN 583: Designing Power Isolation Filters with Ferrite Beads for Altera FPGAs](https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an583.pdf).  If you do not intend to utilize the HPS in the Intel Stratix 10 SX device, you must still provide power to the HPS power supply. Do not leave VCCPLLDIG\_HPS floating or connected to GND. | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑3. HPS Oscillator Clock Input Pin

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| HPS Oscillator Clock Input Pin | | | | |
| Function | Valid Assignment | Schematic Name | Connection Guidelines | Comments / Issues |
| HPS\_OSC\_CLK | Select one of the 48 HPS dedicated I/Os in the Platform Designer HPS Component. |  | Clock input pin that drives the main PLL.  Connect a single-ended clock source to  this pin. The I/O standard of the clock  source must be VCCIO\_HPS compatible.  For more information, refer to the valid  frequency range of the clock source in  the [Intel Stratix 10 Device Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html). | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑4. HPS JTAG Pins

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| HPS JTAG Pins | | | | |
| Function | Valid Assignment | Schematic Name | Connection Guidelines | Comments / Issues |
| JTAG\_TCK | HPS\_IOB\_9 |  | HPS JTAG test clock input pin.  Connect this pin through a 1 kΩ – 10 kΩ pull-down resistor to GND. Do not drive voltage higher than the VCCIO\_HPS supply.  Use the FPGA dedicated JTAG pins as an option to access the HPS JTAG. The option to access the HPS JTAG interface through the FPGA JTAG pins is available in the Intel Quartus Prime Pro Edition. For more details, refer to [AN 802: Intel Stratix 10 SoC Device Design Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683117/20-4/introduction-to-the-soc-device-design.html). | Verify Guidelines have been met or list required actions for compliance. |
| JTAG\_TMS | HPS\_IOB\_10 |  | HPS JTAG test mode select input pin.  Connect this pin to a 1 kΩ – 10 kΩ pull-up resistor to the VCCIO\_HPS supply. Do not drive the voltage higher than the VCCIO\_HPS supply.  Use the FPGA dedicated JTAG pins as an option to access the HPS JTAG. | Verify Guidelines have been met or list required actions for compliance. |
| JTAG\_TDO | HPS\_IOB\_11 |  | HPS JTAG test data output pin.  Use the FPGA dedicated JTAG pins as an option to access the HPS JTAG. | Verify Guidelines have been met or list required actions for compliance. |
| JTAG\_TDI | HPS\_IOB\_12 |  | HPS JTAG test data input pin.  Connect this pin to a 1 kΩ – 10 kΩ pull-up resistor to the VCCIO\_HPS supply. Do not drive the voltage higher than the VCCIO\_HPS supply.  Use the FPGA dedicated JTAG pins as an option to access the HPS JTAG. | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑5. HPS GPIO Pins

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| HPS GPIO Pins | | | | |
| Function | Valid Assignment | Schematic Name | Connection Guidelines | Comments / Issues |
| GPIO0\_IO[0..23] | HPS\_IOA\_[1..24]  HPS\_IOB\_[1..24] |  | General purpose input/output.  Ensure that the I/O standard used is  compatible with the VCCIO\_HPS. | Verify Guidelines have been met or list required actions for compliance. |
| GPIO1\_IO[0..23] |  |

Table 7‑6. HPS SDMMC Pins

1. Intel recommends adding a 1 k? to 10 k? pull-up resistor to every SDMMC data signal that is used.

| HPS SDMMC Pins | | | | | |
| --- | --- | --- | --- | --- | --- |
| Function | Valid Assignment | | Schematic Name | Connection Guidelines | Comments / Issues |
| Group 1 | Group 2 |
| SDMMC\_CCLK | HPS\_IOA\_1 | HPS\_IOB\_15 |  | DMMC clock out. | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_CMD | HPS\_IOA\_2 | HPS\_IOB\_14 |  | SDMMC command line.  Pull this pin high on the board with a weak pull-up resistor. For example, a 10 kΩ to VCCIO\_HPS. | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_DATA0 | HPS\_IOA\_3 | HPS\_IOB\_13 |  | SDMMC Data 0 | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_DATA1 | HPS\_IOA\_4 | HPS\_IOB\_16 |  | SDMMC Data 1 | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_DATA2 | HPS\_IOA\_5 | HPS\_IOB\_17 |  | SDMMC Data 2 | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_DATA3 | HPS\_IOA\_6 | HPS\_IOB\_18 |  | SDMMC Data 3  When using an SD card, there is an existing 50 kΩ pull-up on the SDMMC Data Bit 3, which can be disabled in the HPS software using the SET\_CLR\_CARD\_DETECT  (ACMD42) command. This is not applicable to the eMMC flash. | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_DATA4 | HPS\_IOA\_7 | HPS\_IOB\_19 |  | SDMMC Data 4 | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_DATA5 | HPS\_IOA\_8 | HPS\_IOB\_20 |  | SDMMC Data 5 | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_DATA6 | HPS\_IOA\_9 | HPS\_IOB\_21 |  | SDMMC Data 6 | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_DATA7 | HPS\_IOA\_10 | HPS\_IOB\_22 |  | SDMMC Data 7 | Verify Guidelines have been met or list required actions for compliance. |
| SDMMC\_PWR\_EN | HPS\_IOA\_11 | HPS\_IOB\_23 |  | SDMMC Power Enable | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑7. HPS NAND Pins

| HPS NAND Pins | | | | | |
| --- | --- | --- | --- | --- | --- |
| Function | Valid Assignment | | Schematic Name | Connection Guidelines | Comments / Issues |
| Group 1 | Group 2 |
| NAND\_ADQ0 | HPS\_IOA\_1 | HPS\_IOB\_1 |  | NAND Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ADQ1 | HPS\_IOA\_2 | HPS\_IOB\_2 |  | NAND Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_WE\_N | HPS\_IOA\_3 | HPS\_IOB\_3 |  | NAND Write Enable | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_RE\_N | HPS\_IOA\_4 | HPS\_IOB\_4 |  | NAND Read Enable | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_WP\_N | HPS\_IOA\_5 | HPS\_IOB\_5 |  | NAND Write Protect | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ADQ2 | HPS\_IOA\_6 | HPS\_IOB\_6 |  | NAND Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ADQ3 | HPS\_IOA\_7 | HPS\_IOB\_7 |  | NAND Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_CLE | HPS\_IOA\_8 | HPS\_IOB\_8 |  | NAND Command Latch Enable | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ADQ4 | HPS\_IOA\_9 | HPS\_IOB\_9 |  | NAND Data Bit 4 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ADQ5 | HPS\_IOA\_10 | HPS\_IOB\_10 |  | NAND Data Bit 5 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ADQ6 | HPS\_IOA\_11 | HPS\_IOB\_11 |  | NAND Data Bit 6 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ADQ7 | HPS\_IOA\_12 | HPS\_IOB\_12 |  | NAND Data Bit 7 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ALE | HPS\_IOA\_13 | HPS\_IOB\_13 |  | NAND Address Latch Enable | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_RB | HPS\_IOA\_14 | HPS\_IOB\_14 |  | NAND Ready/Busy  Connect this pin through a pull-up resistor to the VCCIO\_HPS. For more information on the pull-up resistor value, refer to the NAND flash specification. | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_CE\_N | HPS\_IOA\_15 | HPS\_IOB\_15 |  | NAND Chip Enable | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ ADQ8 | HPS\_IOA\_17 | HPS\_IOB\_17 |  | NAND Data Bit 8 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ ADQ9 | HPS\_IOA\_18 | HPS\_IOB\_18 |  | NAND Data Bit 9 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ ADQ10 | HPS\_IOA\_19 | HPS\_IOB\_19 |  | NAND Data Bit 10 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ ADQ11 | HPS\_IOA\_20 | HPS\_IOB\_20 |  | NAND Data Bit 11 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ ADQ12 | HPS\_IOA\_21 | HPS\_IOB\_21 |  | NAND Data Bit 12 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ ADQ13 | HPS\_IOA\_22 | HPS\_IOB\_22 |  | NAND Data Bit 13 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ ADQ14 | HPS\_IOA\_23 | HPS\_IOB\_23 |  | NAND Data Bit 14 | Verify Guidelines have been met or list required actions for compliance. |
| NAND\_ ADQ15 | HPS\_IOA\_24 | HPS\_IOB\_24 |  | NAND Data Bit 15 | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑8. HPS USB Pins

| HPS USB Pins | | | | |
| --- | --- | --- | --- | --- |
| Function | Valid Assignment | Schematic Name | Connection Guidelines | Comments / Issues |
| USB0\_CLK | HPS\_IOA\_1 |  | USB0 Clock | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_STP | HPS\_IOA\_2 |  | USB0 Stop Data | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DIR | HPS\_IOA\_3 |  | USB0 Direction | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DATA0 | HPS\_IOA\_4 |  | USB0 Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DATA1 | HPS\_IOA\_5 |  | USB0 Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_NXT | HPS\_IOA\_6 |  | USB0 Next Data | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DATA2 | HPS\_IOA\_7 |  | USB0 Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DATA3 | HPS\_IOA\_8 |  | USB0 Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DATA4 | HPS\_IOA\_9 |  | USB0 Data Bit 4 | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DATA5 | HPS\_IOA\_10 |  | USB0 Data Bit 5 | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DATA6 | HPS\_IOA\_11 |  | USB0 Data Bit 6 | Verify Guidelines have been met or list required actions for compliance. |
| USB0\_DATA7 | HPS\_IOA\_12 |  | USB0 Data Bit 7 | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_CLK | HPS\_IOA\_13 |  | USB1 Clock | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_STP | HPS\_IOA\_14 |  | USB1 Stop Data | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DIR | HPS\_IOA\_15 |  | USB1 Direction | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DATA0 | HPS\_IOA\_16 |  | USB1 Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DATA1 | HPS\_IOA\_17 |  | USB1 Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_NXT | HPS\_IOA\_18 |  | USB1 Next Data | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DATA2 | HPS\_IOA\_19 |  | USB1 Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DATA3 | HPS\_IOA\_20 |  | USB1 Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DATA4 | HPS\_IOA\_21 |  | USB1 Data Bit 4 | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DATA5 | HPS\_IOA\_22 |  | USB1 Data Bit 5 | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DATA6 | HPS\_IOA\_23 |  | USB1 Data Bit 6 | Verify Guidelines have been met or list required actions for compliance. |
| USB1\_DATA7 | HPS\_IOA\_24 |  | USB1 Data Bit 7 | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑9. HPS EMAC Pins

| HPS EMAC Pins | | | | |
| --- | --- | --- | --- | --- |
| Function | Valid Assignment | Schematic Name | Connection Guidelines | Comments / Issues |
| EMAC0\_TX\_CLK | HPS\_IOA\_13 |  | EMAC0 Transmit Clock | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_TX\_CTL | HPS\_IOA\_14 |  | EMAC0 Transmit Control | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_RX\_CLK | HPS\_IOA\_15 |  | EMAC0 Receive Clock | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_RX\_CTL | HPS\_IOA\_16 |  | EMAC0 Receive Control | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_TXD0 | HPS\_IOA\_17 |  | EMAC0 Transmit Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_TXD1 | HPS\_IOA\_18 |  | EMAC0 Transmit Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_RXD0 | HPS\_IOA\_19 |  | EMAC0 Receive Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_RXD1 | HPS\_IOA\_20 |  | EMAC0 Receive Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_TXD2 | HPS\_IOA\_21 |  | EMAC0 Transmit Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_TXD3 | HPS\_IOA\_22 |  | EMAC0 Transmit Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_RXD2 | HPS\_IOA\_23 |  | EMAC0 Receive Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC0\_RXD3 | HPS\_IOA\_24 |  | EMAC0 Receive Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_TX\_CLK | HPS\_IOB\_1 |  | EMAC1 Transmit Clock | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_TX\_CTL | HPS\_IOB\_2 |  | EMAC1 Transmit Control | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_RX\_CLK | HPS\_IOB\_3 |  | EMAC1 Receive Clock | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_RX\_CTL | HPS\_IOB\_4 |  | EMAC1 Receive Control | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_TXD0 | HPS\_IOB\_5 |  | EMAC1 Transmit Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_TXD1 | HPS\_IOB\_6 |  | EMAC1 Transmit Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_RXD0 | HPS\_IOB\_7 |  | EMAC1 Receive Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_RXD1 | HPS\_IOB\_8 |  | EMAC1 Receive Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_TXD2 | HPS\_IOB\_9 |  | EMAC1 Transmit Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_TXD3 | HPS\_IOB\_10 |  | EMAC1 Transmit Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_RXD2 | HPS\_IOB\_11 |  | EMAC1 Receive Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC1\_RXD3 | HPS\_IOB\_12 |  | EMAC1 Receive Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_TX\_CLK | HPS\_IOB\_13 |  | EMAC2 Transmit Clock | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_TX\_CTL | HPS\_IOB\_14 |  | EMAC2 Transmit Control | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_RX\_CLK | HPS\_IOB\_15 |  | EMAC2 Receive Clock | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_RX\_CTL | HPS\_IOB\_16 |  | EMAC2 Receive Control | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_TXD0 | HPS\_IOB\_17 |  | EMAC2 Transmit Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_TXD1 | HPS\_IOB\_18 |  | EMAC2 Transmit Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_RXD0 | HPS\_IOB\_19 |  | EMAC2 Receive Data Bit 0 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_RXD1 | HPS\_IOB\_20 |  | EMAC2 Receive Data Bit 1 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_TXD2 | HPS\_IOB\_21 |  | EMAC2 Transmit Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_TXD3 | HPS\_IOB\_22 |  | EMAC2 Transmit Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_RXD2 | HPS\_IOB\_23 |  | EMAC2 Receive Data Bit 2 | Verify Guidelines have been met or list required actions for compliance. |
| EMAC2\_RXD3 | HPS\_IOB\_24 |  | EMAC2 Receive Data Bit 3 | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑10. HPS I2C\_EMAC and MDIO Pins

1. The I2C protocol requires pull-up resistors to the VCCIO\_HPS on both, the serial data and the serial clock signals, for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7 k? or lower. The MDIO pin usually requires an external pull-up resistor to the VCCIO\_HPS in the range of 1.0 k? to 4.7 k?.

| HPS I2C\_EMAC and MDIO Pins | | | | | | |
| --- | --- | --- | --- | --- | --- | --- |
| Function | Valid Assignment | | | Schematic Name | Connection Guidelines | Comments / Issues |
| Group 1 | Group 2 | Group 3 |
| I2C\_EMAC2\_SDA | HPS\_IOA\_7 | HPS\_IOB\_9 | HPS\_IOB\_21 |  | I2C EMAC2 Serial Data | Verify Guidelines have been met or list required actions for compliance. |
| I2C\_EMAC2\_SCL | HPS\_IOA\_8 | HPS\_IOB\_10 | HPS\_IOB\_22 |  | I2C EMAC2 Serial Clock | Verify Guidelines have been met or list required actions for compliance. |
| I2C\_EMAC1\_SDA | HPS\_IOA\_9 | HPS\_IOB\_19 | - |  | I2C EMAC1 Serial Data | Verify Guidelines have been met or list required actions for compliance. |
| I2C\_EMAC1\_SCL | HPS\_IOA\_10 | HPS\_IOB\_20 | - |  | I2C EMAC1 Serial Clock | Verify Guidelines have been met or list required actions for compliance. |
| I2C\_EMAC0\_SDA | HPS\_IOA\_11 | HPS\_IOB\_11 | HPS\_IOB\_23 |  | I2C EMAC0 Serial Data | Verify Guidelines have been met or list required actions for compliance. |
| I2C\_EMAC0\_SCL | HPS\_IOA\_12 | HPS\_IOB\_12 | HPS\_IOB\_24 |  | I2C EMAC0 Serial Clock | Verify Guidelines have been met or list required actions for compliance. |
| MDIO2\_MDIO | HPS\_IOA\_7 | HPS\_IOB\_9 | - |  | EMAC2 MDIO | Verify Guidelines have been met or list required actions for compliance. |
| MDIO2\_MDC | HPS\_IOA\_8 | HPS\_IOB\_10 | - |  | EMAC2 MDC | Verify Guidelines have been met or list required actions for compliance. |
| MDIO1\_MDIO | HPS\_IOA\_9 | HPS\_IOB\_19 | - |  | EMAC1 MDIO | Verify Guidelines have been met or list required actions for compliance. |
| MDIO1\_MDC | HPS\_IOA\_10 | HPS\_IOB\_20 | - |  | EMAC1 MDC | Verify Guidelines have been met or list required actions for compliance. |
| MDIO0\_MDIO | HPS\_IOA\_11 | HPS\_IOB\_11 | HPS\_IOB\_23 |  | EMAC0 MDIO | Verify Guidelines have been met or list required actions for compliance. |
| MDIO0\_MDC | HPS\_IOA\_12 | HPS\_IOB\_12 | HPS\_IOB\_24 |  | EMAC0 MDC | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑11. HPS I2C Pins

1. The I2C protocol requires pull-up resistors to the VCCIO\_HPS on both, the serial data and the serial clock signals, for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7 k? or lower.

| HPS I2C Pins | | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Function | Valid Assignment | | | | Schematic Name | Connection Guidelines | Comments / Issues |
| Group 1 | Group 2 | Group 3 | Group 4 |
| I2C0\_SDA | HPS\_IOA\_5 | HPS\_IOA\_23 | HPS\_IOB\_3 | - |  | I2C0 Serial Data | Verify Guidelines have been met or list required actions for compliance. |
| I2C0\_SCL | HPS\_IOA\_6 | HPS\_IOA\_24 | HPS\_IOB\_4 | - |  | I2C0 Serial Clock | Verify Guidelines have been met or list required actions for compliance. |
| I2C1\_SDA | HPS\_IOA\_3 | HPS\_IOA\_21 | HPS\_IOB\_7 | HPS\_IOB\_13 |  | I2C1 Serial Data | Verify Guidelines have been met or list required actions for compliance. |
| I2C1\_SCL | HPS\_IOA\_4 | HPS\_IOA\_22 | HPS\_IOB\_8 | HPS\_IOB\_14 |  | I2C1 Serial Clock | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑12. HPS SPI Pins

| HPS SPI Pins | | | | | | |
| --- | --- | --- | --- | --- | --- | --- |
| Function | Valid Assignment | | | Schematic Name | Connection Guidelines | Comments / Issues |
| Group 1 | Group 2 | Group 3 |
| SPIM0\_CLK | HPS\_IOA\_5 | HPS\_IOB\_21 | HPS\_IOB\_21 |  | SPIM0 Clock | Verify Guidelines have been met or list required actions for compliance. |
| SPIM0\_MOSI | HPS\_IOA\_6 | HPS\_IOB\_22 | HPS\_IOB\_22 |  | SPIM0 Master Out Slave In | Verify Guidelines have been met or list required actions for compliance. |
| SPIM0\_MISO | HPS\_IOA\_7 | HPS\_IOB\_19 | HPS\_IOB\_23 |  | SPIM0 Master In Slave Out | Verify Guidelines have been met or list required actions for compliance. |
| SPIM0\_SS0\_N | HPS\_IOA\_8 | HPS\_IOB\_20 | HPS\_IOB\_24 |  | SPIM0 Slave Select 0 | Verify Guidelines have been met or list required actions for compliance. |
| SPIM0\_SS1\_N | HPS\_IOA\_1 | HPS\_IOB\_18 | HPS\_IOB\_18 |  | SPIM0 Slave Select 1 | Verify Guidelines have been met or list required actions for compliance. |
| SPIM1\_CLK | HPS\_IOA\_9 | HPS\_IOA\_21 | HPS\_IOB\_1 |  | SPIM1 Clock | Verify Guidelines have been met or list required actions for compliance. |
| SPIM1\_MOSI | HPS\_IOA\_10 | HPS\_IOA\_22 | HPS\_IOB\_2 |  | SPIM1 Master Out Slave In | Verify Guidelines have been met or list required actions for compliance. |
| SPIM1\_MISO | HPS\_IOA\_11 | HPS\_IOA\_23 | HPS\_IOB\_3 |  | SPIM1 Master In Slave Out | Verify Guidelines have been met or list required actions for compliance. |
| SPIM1\_SS0\_N | HPS\_IOA\_12 | HPS\_IOA\_24 | HPS\_IOB\_4 |  | SPIM1 Slave Select 0 | Verify Guidelines have been met or list required actions for compliance. |
| SPIM1\_SS1\_N | HPS\_IOA\_2 | HPS\_IOA\_20 | HPS\_IOB\_5 |  | SPIM1 Slave Select 1 | Verify Guidelines have been met or list required actions for compliance. |
| SPIS0\_CLK | HPS\_IOA\_1 | HPS\_IOA\_21 | HPS\_IOB\_9 |  | SPIS0 Clock | Verify Guidelines have been met or list required actions for compliance. |
| SPIS0\_MOSI | HPS\_IOA\_2 | HPS\_IOA\_22 | HPS\_IOB\_10 |  | SPIS0 Master Out Slave In | Verify Guidelines have been met or list required actions for compliance. |
| SPIS0\_MISO | HPS\_IOA\_4 | HPS\_IOA\_24 | HPS\_IOB\_12 |  | SPIS0 Master In Slave Out | Verify Guidelines have been met or list required actions for compliance. |
| SPIS0\_SS0\_N | HPS\_IOA\_3 | HPS\_IOA\_23 | HPS\_IOB\_11 |  | SPIS0 Slave Select 0 | Verify Guidelines have been met or list required actions for compliance. |
| SPIS1\_CLK | HPS\_IOA\_9 | HPS\_IOB\_5 | HPS\_IOB\_21 |  | SPIS1 Clock | Verify Guidelines have been met or list required actions for compliance. |
| SPIS1\_MOSI | HPS\_IOA\_10 | HPS\_IOB\_6 | HPS\_IOB\_22 |  | SPIS1 Master Out Slave In | Verify Guidelines have been met or list required actions for compliance. |
| SPIS1\_MISO | HPS\_IOA\_12 | HPS\_IOB\_8 | HPS\_IOB\_24 |  | SPIS1 Master In Slave Out | Verify Guidelines have been met or list required actions for compliance. |
| SPIS1\_SS0\_N | HPS\_IOA\_11 | HPS\_IOB\_7 | HPS\_IOB\_23 |  | SPIS1 Slave Select 0 | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑13. HPS UART Pins

| HPS UART Pins | | | | | | |
| --- | --- | --- | --- | --- | --- | --- |
| Function | Valid Assignment | | | Schematic Name | Connection Guidelines | Comments / Issues |
| Group 1 | Group 2 | Group 3 |
| UART0\_CTS\_N | HPS\_IOA\_1 | HPS\_IOA\_21 | HPS\_IOB\_1 |  | UART0 Clear to Send | Verify Guidelines have been met or list required actions for compliance. |
| UART0\_RTS\_N | HPS\_IOA\_2 | HPS\_IOA\_22 | HPS\_IOB\_2 |  | UART0 Request to Send | Verify Guidelines have been met or list required actions for compliance. |
| UART0\_TX | HPS\_IOA\_3 | HPS\_IOA\_23 | HPS\_IOB\_3 |  | UART0 Transmit | Verify Guidelines have been met or list required actions for compliance. |
| UART0\_RX | HPS\_IOA\_4 | HPS\_IOA\_24 | HPS\_IOB\_4 |  | UART0 Receive | Verify Guidelines have been met or list required actions for compliance. |
| UART1\_CTS\_N | HPS\_IOA\_5 | HPS\_IOB\_5 | HPS\_IOB\_17 |  | UART1 Clear to Send | Verify Guidelines have been met or list required actions for compliance. |
| UART1\_RTS\_N | HPS\_IOA\_6 | HPS\_IOB\_6 | HPS\_IOB\_18 |  | UART1 Request to Send | Verify Guidelines have been met or list required actions for compliance. |
| UART1\_TX | HPS\_IOA\_7 | HPS\_IOB\_7 | HPS\_IOB\_15 |  | UART1 Transmit | Verify Guidelines have been met or list required actions for compliance. |
| UART1\_RX | HPS\_IOA\_8 | HPS\_IOB\_8 | HPS\_IOB\_16 |  | UART1 Receive | Verify Guidelines have been met or list required actions for compliance. |

Table 7‑14. HPS Trace Pins

| HPS UART Pins | | | | |
| --- | --- | --- | --- | --- |
| Function | Valid Assignment | Schematic Name | Connection Guidelines | Comments / Issues |
| Trace\_CLK | HPS\_IOA\_20 |  | Trace Clock | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_20 |
| Trace\_D0 | HPS\_IOA\_21 |  | Trace Data 0 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_21 |
| Trace\_D1 | HPS\_IOA\_22 |  | Trace Data 1 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_22 |
| Trace\_D2 | HPS\_IOA\_23 |  | Trace Data 2 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_23 |
| Trace\_D3 | HPS\_IOA\_24 |  | Trace Data 3 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_24 |
| Trace\_D4 | HPS\_IOA\_19 |  | Trace Data 4 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOA\_7 |
| HPS\_IOB\_19 |
| HPS\_IOB\_7 |
| Trace\_D5 | HPS\_IOA\_18 |  | Trace Data 5 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOA\_6 |
| HPS\_IOB\_18 |
| HPS\_IOB\_6 |
| Trace\_D6 | HPS\_IOA\_17 |  | Trace Data 6 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOA\_5 |
| HPS\_IOB\_17 |
| HPS\_IOB\_5 |
| Trace\_D7 | HPS\_IOA\_16 |  | Trace Data 7 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOA\_4 |
| HPS\_IOB\_16 |
| HPS\_IOB\_4 |
| Trace\_D8 | HPS\_IOA\_15 |  | Trace Data 8 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOA\_3 |
| HPS\_IOB\_15 |
| HPS\_IOB\_3 |
| Trace\_D9 | HPS\_IOA\_14 |  | Trace Data 9 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOA\_2 |
| HPS\_IOB\_14 |
| HPS\_IOB\_2 |
| Trace\_D10 | HPS\_IOA\_13 |  | Trace Data 10 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOA\_1 |
| HPS\_IOB\_13 |
| HPS\_IOB\_1 |
| Trace\_D11 | HPS\_IOA\_12 |  | Trace Data 11 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_12 |
| Trace\_D12 | HPS\_IOA\_11 |  | Trace Data 12 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_11 |
| Trace\_D13 | HPS\_IOA\_10 |  | Trace Data 13 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_10 |
| Trace\_D14 | HPS\_IOA\_9 |  | Trace Data 14 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_9 |
| Trace\_D15 | HPS\_IOA\_8 |  | Trace Data 15 | Verify Guidelines have been met or list required actions for compliance. |
| HPS\_IOB\_8 |

### Notes on HPS Pins

1. Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime Software checks your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, packaging, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Intel Stratix 10 GX device variant.
2. Select the capacitance values for the power supply after considering the amount of power needed to supply over the frequency of operation of the circuit being decoupled. Calculate the target impedance for the power plane based on the current draw and voltage drop requirements of the device/supply. Decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to the “Equivalent Series Inductance” of the mounting of the packages. Consider proper board design techniques, such as interplane capacitance with low inductance for higher frequency decoupling. Refer to the PDN tool.
3. Use the Intel Stratix 10 Early Power Estimator (EPE) to determine the preliminary current requirements for the VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
4. These supplies may share power planes across multiple Intel Stratix 10 devices.
5. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
6. The Low Noise Switching Regulator is a switching regulator circuit encapsulated in a thin surface mount package, containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz, and has a fast transient response. The switching frequency range is not an Intel requirement.
7. The number of modular I/O banks on Intel Stratix 10 devices depends on the device density. For the indexes available for a specific device, refer to the I/O Bank section in the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683518/21-2/i-o-overview.html).
8. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires that the AC-coupling capacitor is placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
9. For item [#], refer to the device pin table for the pin-out mapping.
10. The peripheral pins are programmable through pin multiplexors. Each pin may have multiple functions. HPS and SDM dedicated I/O pin multiplexing is programmable using the Intel Quartus Prime Software. The pin mux determines how the pins are used.
11. These pins are inverted or active-low signals.
12. Example 3 through Example 6 in the Intel Stratix 10 Device Family Pin Connection Guidelines illustrate the power supply sharing guidelines for the Intel Stratix 10 SX devices.

# External Memory Interfaces

Table 8‑1. Reference Documents

|  |
| --- |
| Document |
| [Intel Stratix 10 Recommended Reference Literature](https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/docs.html) |
| [Intel Stratix 10 Pin Out Files](https://www.intel.com/content/www/us/en/support/programmable/support-resources/devices/lit-dp.html#stratix-10) |
| [Intel Stratix 10 Device Family Pin Connection Guidelines](https://www.intel.com/content/www/us/en/docs/programmable/683028/current/device-family-pin-connection-guidelines.html) |
| [Board Developer Center](https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-guidance/board-developer.html) |
| [Intel Stratix 10 External Memory Interfaces User Guide (PDF)](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/ug-s10-emi.pdf) |
| [Board Skew Parameters Tool](https://www.intel.com/content/www/us/en/programmable/solutions/technology/memory/estimator/board-skew.html) |
| [External Memory Interface Pin Information for Intel Stratix 10 Devices](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/dp/stratix-10/stratix10emif.pdf) |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| DDR4 IO Bank | VCCIO Voltage | DDR4 VDD/VDDQ Voltage | DDR4 VPP | VREF | VTT |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| QDRIV IO Bank | VCCIO Voltage | QDRIV VDD Voltage | QDRIV VDDQ Voltage | VREF | VTT |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

Table 8‑2. External Memory Interface Pins

| External Memory Interface Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| DQS[0:47]  DQS[48:95] |  | Optional data strobe signal used in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry.  Connect unused pins as defined in the Intel Quartus Prime Software. | Verify Guidelines have been met or list required actions for compliance. |
| DQSn[0:47] DQSn[48:95] |  | Optional complementary data strobe signal used in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry.  Connect unused pins as defined in the Intel Quartus Prime Software. | Verify Guidelines have been met or list required actions for compliance. |
| DQ[0:47]  DQ[48:95] |  | Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, if you plan to migrate to a different memory interface that has a different DQ bus width, you need to re-evaluate your pin assignments. Analyze the available DQ pins across all pertinent DQS columns in the device pin-out file.  Connect unused pins as defined in the Intel Quartus Prime Software. | Verify Guidelines have been met or list required actions for compliance. |

Table 8‑3. Part A: DDR3 Interface Pins

| Part A: DDR3 Interface Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Data pin - DQ |  | Place on DQ pins which are in DQS groups located in suitable IOBANKS, relative to the address/command IOBANK. Refer to the generated IP readme.txt file for an example pin-out.  Additional HPS pin-out requirements:  Refer to the Hard Processor Subsystem DQS group placement information in the External Memory Interfaces Intel Stratix 10 FPGA IP User Guide. | Verify Guidelines have been met or list required actions for compliance. |
| Data strobe – DQS/DQSn |  | Place on DQS pins which are in DQS groups located in suitable IOBANKS, relative to the address/command IOBANK. Refer to the generated IP readme.txt file for an example pin-out.  Additional HPS pin-out requirements:  Refer to the Hard Processor Subsystem DQS group placement information in the External Memory Interfaces Intel Stratix 10 FPGA IP User Guide. | Verify Guidelines have been met or list required actions for compliance. |
| DM |  | Place on DM pins which are in DQS groups located in suitable IOBANKS, relative to the address/command IOBANK. Refer to the generated IP readme.txt file for an example pin-out.  Additional HPS pin-out requirements:  Refer to the Hard Processor Subsystem DQS group placement information in the External Memory Interfaces Intel Stratix 10 FPGA IP User Guide. | Verify Guidelines have been met or list required actions for compliance. |
| mem\_clk and mem\_clk\_n |  | Place it on CK/CK\_N pins in the address/command IOBANK as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  Additional HPS pin-out requirements:  mem\_clk and mem\_clk\_n must be placed in IO bank 2M. | Verify Guidelines have been met or list required actions for compliance. |
| clock\_source |  | Place it on a PLL reference clock pin in one of the IOBANKS used by the memory interface. Refer tothe generated IP readme.txt file for an example pinout.  Additional HPS pinout requirements:  Clock source must be placed in IO bank 2M  Intel does not check these but listed below are important recommendations for the clock source:  1) Use one of the recommended frequencies shown in the IP (IP General tab -> Clocks),  2) Use a low jitter clock source. Refer to the recommendations for Memory Output Clock Jitter in the [Intel Stratix 10 Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html). | Verify Guidelines have been met or list required actions for compliance. |
| Address [BA, A] |  | Place it on address pins in the address/command IOBANK as specified in the <variation\_name>\_readme.txt file,generated with your IP.  Additional HPS pinout requirements:  Address pins must be placed in IO bank 2M. | Verify Guidelines have been met or list required actions for compliance. |
| Command [CKE, ODT, CS\_N, RAS, CAS, WE\_N] |  | Place it on command pins in the address/command IOBANK as specified in the <variation\_name>\_readme.txt file, generated with your IP.  Additional HPS pinout requirements:  Command pins must be placed in IO bank 2M. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for DDR3 Memory |  | Place it on the mem\_reset\_n pin in the address/command IOBANK as specified in the <variation\_name>\_readme.txt file,generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for DDR3 Controller |  | Any user IO pins. The reset pin can alternatively be generated internally. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ\_[#] |  | Used when calibrated OCT for memory interface pins is implemented.  Place it on an RZQ pin in one of the IOBANKS used by the memory interface. Refer to the generated IP readme.txt file for an example pinout.  Additional HPS pinout requirements:  RZQ must be placed in IO bank 2M. | Verify Guidelines have been met or list required actions for compliance. |
| Multiple DDR3 IP placed in an IO column  Clock\_source RZQ DQ/DM/DQS Address/command/  mem\_clk |  | Check the latest pin-out rules for sharing resources between multiple interfaces in the same IO column including:  -Check that the interfaces are compatible for resource sharing  -pll ref clock and core clock sharing  -RZQ  -IOBANKS and placement of address/command/clk signals and data groups.  Do not share any resources between HPS and non-HPS DDR3 interfaces | Verify Guidelines have been met or list required actions for compliance. |

1. DDR3 supports only differential DQS signaling.

**Additional Comments:** Check vendor datasheet to make sure x4 DQS configuration is not being used since it is currently not supported.

Table 8‑4. Part B: DDR3 Interface Termination Guidelines

| Part B: DDR3 Interface Termination Guidelines | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Memory clocks@ Memory |  | Fly by termination scheme. Clock signals are already terminated on the DIMM. No need to put any termination on the board.  Discrete Devices – Fly by termination scheme. Differential termination resistor needs to be included in the design. Depending on your board stack-up and layout requirements, choose your differential termination resistor value. | Verify Guidelines have been met or list required actions for compliance. |
| Memory clocks@ FPGA |  | Use series output termination with calibration.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| DQS @ Memory  DQ @ Memory  DM @ Memory |  | Use ODT.  If DM pins are unused, refer to the DDR3/DDR3L manufacturer's data sheet for connection recommendations. Typically, they must be tied low, using a resistor no greater than 4 \*Rtt (the nominal ODT value used on the memory device). | Verify Guidelines have been met or list required actions for compliance. |
| DQS @ FPGA  DQ @ FPGA |  | Use series output termination with calibration and parallel input termination with calibration  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| DM @ FPGA |  | Use series output termination with calibration.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Address [BA, A] @ Memory |  | DIMM - Fly by termination scheme. Address signals are already terminated on the DIMM. No need to put any termination on the board.  Discrete Device – Fly by termination scheme. Terminated at the device. | Verify Guidelines have been met or list required actions for compliance. |
| Address [BA, A] @ FPGA |  | Use fast slew rate and serial output termination with calibration.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Command [CKE, ODT, CS\_N, RAS, CAS, WE\_N] @ Memory |  | DIMM implementation - Fly by termination scheme. Command signals are already terminated on the DIMM. No need to put any termination on the board.  Discrete Device – Fly by termination scheme. Terminated at the device. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for DDR3 Memory |  | For DDR3, use 1.5 V and fast slew rate.  Also use serial output termination with calibration for SSTL-15 DDR3.  For DDR3L, use SSTL-135, fast slew rate and serial output termination.  Check the FPGA termination value in the .qip file, generated with your IP.  It is not recommended to externally terminate this reset to Vtt. | Verify Guidelines have been met or list required actions for compliance. |
| Command [CKE, ODT, CS\_N, RAS, CAS, WE\_N] @ FPGA |  | Use fast slew rate and serial output termination with calibration.  Check the termination value in the .qip file, generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |

1. The termination schemes suggested in the table are general guidelines. Perform a board level simulation for your particular system/board to determine optimal termination scheme.

**Additional Comments:**

Table 8‑5. Miscellaneous

|  |  |  |  |
| --- | --- | --- | --- |
| Miscellaneous | | | |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Vref |  | Use a voltage regulator to generate this voltage. | Verify Guidelines have been met or list required actions for compliance. |
| Vtt |  | Use a voltage regulator to generate this voltage.  Typically, DDR3 DIMMS have decoupling capacitors connected between the VTT and VDD (1.5 V), and it is recommended that designers follow this approach. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ\_[#] |  | RZQ pin is connected to GND through an external 240 Ω or 100 Ω ±1% resistor. Refer to the [Intel Stratix 10 General Purpose I/O User Guide](https://www.altera.com/documentation/sam1438349166154.html) for the OCT impedance options for the desired OCT scheme. | Verify Guidelines have been met or list required actions for compliance. |

**Additional Comments:**

Table 8‑6. Part C: DDR4 Interface Pins

| Part C: DDR4 Interface Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Data pin - DQ |  | Place on DQ pins which are in DQS groups located in suitable IOBANKS relative to the address/command IOBANK. Refer to the generated IP readme.txt file for an example pin-out.  Additional HPS pin-out requirements:  Refer to the Hard Processor Subsystem DQS group placement information in the [External Memory Interfaces Intel Stratix 10 FPGA IP User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683741/21-3-19-2-4/release-information.html). | Verify Guidelines have been met or list required actions for compliance. |
| Data strobe - DQS/DQSn |  | Place on DQS pins that are in DQS groups located in suitable IOBANKS relative to the address/command IOBANK. Refer to the generated IP readme.txt file for an example pin-out.  Additional HPS pin-out requirements:  Refer to the Hard Processor Subsystem DQS group placement information in the [External Memory Interfaces Intel Stratix 10 FPGA IP User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683741/21-3-19-2-4/release-information.html). | Verify Guidelines have been met or list required actions for compliance. |
| mem\_clk and mem\_clk\_n |  | Place it on the CK/CK\_N pins in the address/command IOBANK as specified in the <variation\_name>\_readme.txt file, generated with your IP.  Additional HPS pin-out requirements:  mem\_clk and mem\_clk\_n must be placed in IO bank 2M. | Verify Guidelines have been met or list required actions for compliance. |
| clock\_source |  | Place it on a PLL reference clock pin in one of the IOBANKS used by the memory interface. Refer to the generated IP readme.txt file for an example pin-out.  Additional HPS pin-out requirements:  Clock source must be placed in IO bank 2M.  Intel does not check these but listed below are important recommendations for the clock source:  1) Use one of the recommended frequencies shown in the IP (IP General tab -> Clocks),  2) Use a low jitter clock source. See the recommendations for Memory Output Clock Jitter in the [Intel Stratix 10 Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html). | Verify Guidelines have been met or list required actions for compliance. |
| DBI\_n |  | Place on DBI\_n pins, which are in DQS groups located in suitable IOBANKS relative to the address/command IOBANK. See the generated IP readme.txt file for an example pin-out.  Additional HPS pin-out requirements:  Refer to the Hard Processor Subsystem DQS group placement information in the [External Memory Interfaces Intel Stratix 10 FPGA IP User Guide](https://www.intel.com/content/www/us/en/docs/programmable/683741/21-3-19-2-4/release-information.html). | Verify Guidelines have been met or list required actions for compliance. |
| Address [BA,BG, A] |  | Place it on address pins in the address/command IOBANK as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  Additional HPS pin-out requirements:  Address pins must be placed in IO bank 2M. | Verify Guidelines have been met or list required actions for compliance. |
| Command [CKE, ODT, CS\_N, ACT\_n, PAR] |  | Place it on command pins in the address/command IOBANK as specified in the <variation\_name>\_readme.txt file, generated with your IP.  Additional HPS pin-out requirements:  Command pins must be placed in IO bank 2M. | Verify Guidelines have been met or list required actions for compliance. |
| ALERT\_n |  | Alert input that indicates to the system's memory controller that a specific alert or event has occurred.  Place it on the mem\_alert\_n pin as specified in the <variation\_name>\_readme.txt file, generated with your IP. This may be in a DQS group or in the address/command IOBANK.  Additional HPS pin-out requirements:  Recommended placement is in IO bank 2N lanes 0 or 1. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for DDR4 Memory |  | Place it on the mem\_reset\_n pin in the address/command IOBANK as specified in the <variation\_name>\_readme.txt file, generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for DDR4  controller |  | Any user IO pins. The reset pin can alternatively be generated internally. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ\_[#] |  | Used when calibrated OCT for the memory interface pins is implemented.  Place it on an RZQ pin in one of the IOBANKS used by the memory interface. Refer to the generated IP readme.txt file for an example pin-out.  Additional HPS pin-out requirements:  RZQ must be placed in IO bank 2M. | Verify Guidelines have been met or list required actions for compliance. |
| Multiple DDR4 IP placed in an IO column  Clock\_source RZQ DQ/DM/DQS Address/command/  mem\_clk |  | Check the latest pin-out rules for sharing resources between multiple interfaces in the same IO column including: - Check that the interfaces are compatible for resource sharing - pll ref clock and core clock sharing - RZQ - IOBANKS and placement of address/command/clk signals and data groups.  Do not share any resources between HPS and non-HPS DDR4 interfaces. | Verify Guidelines have been met or list required actions for compliance. |

1. DDR4 supports only differential DQS signaling.

**Additional Comments:** Check vendor datasheet to make sure x4 DQS configuration is not being used since it is currently not supported.

Table 8‑7. Part D: DDR4 Interface Termination Guidelines

| Part D: DDR4 Interface Termination Guidelines | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Memory clocks@ Memory |  | Fly by termination scheme. Clock signals are already terminated on the DIMM. No need to put any termination on the board.  Devices – Fly by termination scheme. differential termination resistor needs to be included in the design. Depending on your board stack-up and layout requirements, choose your differential termination resistor value. | Verify Guidelines have been met or list required actions for compliance. |
| Memory clocks@ FPGA |  | Use series output termination with calibration.  Check the termination value in the .qip file  which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| DQS @ Memory  DQ @ Memory  DBI\_n @ Memory |  | Use ODT. | Verify Guidelines have been met or list required actions for compliance. |
| DQS @ FPGA  DQ @ FPGA  DBI\_n@ FPGA |  | Use series output termination with calibration and parallel input termination with calibration  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Address [BA,BG, A] @ Memory |  | DIMM - Fly by termination scheme. Address signals are already terminated on the DIMM. No need to put any termination on the board.  Discrete Device – Fly by termination scheme. Terminated at the device. | Verify Guidelines have been met or list required actions for compliance. |
| Address [BA, BG, A] @ FPGA |  | Use fast slew rate and serial output termination with calibration.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Command [CKE, ODT, CS\_N, ACT\_n, PAR] @ Memory |  | DIMM implementation - Fly by termination scheme. Command signals are already terminated on the DIMM. No need to put any termination on the board.  Discrete Device – Fly by termination scheme. Terminated at the device. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for DDR4 Memory |  | Use 1.2 V I/O standard to meet the 1.2 V CMOS logic levels on the DDR4 device or DIMM.  Check the termination value in the .qip file which is generated with your IP.  It is not recommended to terminate this reset to Vtt. | Verify Guidelines have been met or list required actions for compliance. |
| ALERT\_n |  | Use an external pull-up resistor (typically 10 kΩ) to VDD (1.2 V). | Verify Guidelines have been met or list required actions for compliance. |
| Command [CKE, ODT, CS\_N, ACT\_n, PAR] @ FPGA |  | Termination with calibration.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |

1. The termination schemes suggested in the table are general guidelines. Perform board level simulation for your particular system/board to determine optimal termination scheme.

**Additional Comments:**

Table 8‑8. Miscellaneous

| Miscellaneous | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Vref |  | Use a voltage regulator to generate this voltage.  The DDR4 memory device requires a Vref of VDD/2 (0.6 V) connected to its VREFCA pins.  The DDR4 memory device VREFDQ is generated internally.  The FPGA DDR4 interface IOBANKS Vref is generated internally for the DQ, DQS, DQS\_n and DBI\_n signals. | Verify Guidelines have been met or list required actions for compliance. |
| Vtt |  | Use a voltage regulator to generate this voltage.  Typically, DDR4 DIMMS have decoupling capacitors connected between VTT and VDD (1.2 V), and it is recommended that designers follow this approach. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ\_[#] |  | RZQ pin is connected to GND through an external 240 Ω or 100 Ω ±1% resistor. Use the value specified in the IP. | Verify Guidelines have been met or list required actions for compliance. |

**Additional Comments:**

Table 8‑9. Part E: RLDRAM II/3 Interface Pins

| Part E: RLDRAM II/3 Interface Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Data pin - DQ |  | Place it on DQ pins of the DQ/DQS group.  The order of the DQ bits within a designated DQ group/bus is not important. Place the DQ pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| DM |  | Place on the DQ pins of the applicable DQ/DQS pin group. Place it on DM pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| QVLD |  | Place on a DQ pin in the same bank as the read data. Intel IP does not use the QVLD pin. You can leave this pin unconnected on your board. You may not be able to fit these pins in a DQS group. | Verify Guidelines have been met or list required actions for compliance. |
| Read clock to the FPGA - QK/QKn |  | Place on the corresponding DQS and DQSn pins of the DQ/DQS group. Please use the <variation\_name>\_readme.txt file which is generated with your IP as a guideline. | Verify Guidelines have been met or list required actions for compliance. |
| Write clock from the FPGA - DK/DKn |  | Place DK pins in the same IO bank as the read clock (QK) pins & DQ pins in that byte lane. Please use the <variation\_name>\_readme.txt file which is generated with your IP as a guideline.  DK/DK# must use differential output-capable pins. | Verify Guidelines have been met or list required actions for compliance. |
| Memory clock – CK/CKn |  | Place it on CK/CKn pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| clock\_source |  | Place it on “PLL\_REF\_CLK” pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. Use a frequency recommended by the EMIF RLDRAM 3 IP GUI. | Verify Guidelines have been met or list required actions for compliance. |
| Address  A, BA |  | Place it on Address/ Bank Address pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Command  CS#, REF#, WE# |  | Place it on Command pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for RLDRAM Memory  (RLDRAM 3 only) |  | Place the RESET signal as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for RLDRAM Controller |  | Any user IO pin. The reset pin can alternatively be generated internally. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ |  | Used when calibrated OCT for the memory interface pins is implemented.  Place it on RZQ pin as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |

**Additional Comments:**

Table 8‑10. Part F: RLDRAM II/ 3 Interface Termination Guidelines

| Part F: RLDRAM II/ 3 Interface Termination Guidelines | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Write Clock (DK/DKn) @ FPGA |  | Use series termination with calibration as output termination. Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Write Clock (DK/DKn) @ Memory |  | RLDRAM 3: Use ODT. | Verify Guidelines have been met or list required actions for compliance. |
| Read Clock (QK/QKn) @ FPGA |  | Use parallel termination with calibration as input termination.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Read Clock (QK/QKn) @ Memory |  | Read clock output impedance is implemented with the help of the RLDRAM II /3 component ZQ input pin on the memory device side. If not, you may need to put a 50 Ω series termination on the memory side. | Verify Guidelines have been met or list required actions for compliance. |
| Memory clocks @ Memory |  | Use a differential termination.  Depending on your board stack-up and layout requirements, choose your differential termination resistor value. | Verify Guidelines have been met or list required actions for compliance. |
| Memory clocks @ FPGA |  | Use series output termination without calibration.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| DQ @ Memory |  | Use ODT. | Verify Guidelines have been met or list required actions for compliance. |
| DQ @ FPGA |  | Use Dynamic OCT, which is parallel input termination with calibration and series output termination.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| DM @ Memory |  | Use ODT. | Verify Guidelines have been met or list required actions for compliance. |
| DM @ FPGA |  | Use series output termination.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| QVLD @ Memory |  | Read clock output impedance is implemented with the help of the RLDRAM II /3 component ZQ input pin on the memory device side. If not, you may need to put a 50 Ω series termination on the memory side. | Verify Guidelines have been met or list required actions for compliance. |
| QVLD @ FPGA |  | If connected, use parallel input termination with calibration. | Verify Guidelines have been met or list required actions for compliance. |
| Address [BA, A] @ Memory |  | Parallel termination to VTT is recommended.  Micron technical note TN-44-01 (RLDRAM 3 Design Guide), indicates that it may be possible to achieve adequate signal integrity without signal terminations at lower frequencies and with short PCB traces. Simulations should be performed to determine the termination requirements. | Verify Guidelines have been met or list required actions for compliance. |
| Address [BA, A] @ FPGA |  | If there are multiple loads on certain FPGA output pins (for example, if the address bus is shared across several memory devices), use of maximum drive strength setting may be preferred over the series OCT setting. Use board level simulations to pick the optimal setting for the best signal integrity. | Verify Guidelines have been met or list required actions for compliance. |
| Command [CS#,WE#, REF#] @ Memory |  | REF#, WE#: Parallel termination to VTT is recommended.  CS#: Use either parallel termination to VTT or a pull-up to VDD. Refer to the memory vendor’s RLDRAM II/3 component data sheet for further information. | Verify Guidelines have been met or list required actions for compliance. |
| Command [CKE, CS\_N, RAS, CAS, WE\_N] @ FPGA |  | If there are multiple loads on certain FPGA output pins (for example, if the address bus is shared across several memory devices), use of maximum drive strength setting may be preferred over the series OCT setting. Use board level simulations to pick the optimal setting for the best signal integrity. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for RLDRAM Memory  (RLDRAM 3 only) |  | Use SSTL-12 Class I I/O standard to meet the CMOS logic levels on the RLDRAM 3 device.  Use a pull-down resistor to GND. Typical value is 10 kΩ, but you should select a suitable value for your implementation.  Refer to the memory vendor’s RLDRAM II/3 component data sheet for further information. | Verify Guidelines have been met or list required actions for compliance. |

1. The termination schemes suggested in the table are general guidelines. Perform board level simulation for your particular system/board to determine optimal termination scheme.

**Additional Comments:**

Table 8‑11. Miscellaneous

|  |  |  |  |
| --- | --- | --- | --- |
| Miscellaneous | | | |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Vref |  | Use a voltage regulator to generate this voltage. | Verify Guidelines have been met or list required actions for compliance. |
| Vtt |  | Use a voltage regulator to generate this voltage. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ |  | RZQ pin is connected to GND through an external 240 Ω or 100 Ω ±1% resistor. Refer to the [Intel Stratix 10 General Purpose I/O User Guide](https://www.altera.com/documentation/sam1438349166154.html) for the OCT impedance options for the desired OCT scheme. | Verify Guidelines have been met or list required actions for compliance. |

**Additional Comments:**

Table 8‑12. Part G: QDR II/II+/Xtreme Interface Pins

| Part G: QDR II/II+/Xtreme Interface Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Q – Read data pins |  | Place it on Q pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  The order of the Q bits within a designated DQ group/bus is not important. | Verify Guidelines have been met or list required actions for compliance. |
| D – Write data pins |  | Place it on D pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  The order of the D bits within a designated DQ group/bus is not important. | Verify Guidelines have been met or list required actions for compliance. |
| Read clock to the FPGA - CQ/CQn |  | Place it on CQ/CQN pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Write clock from the FPGA - K/Kn |  | Place it on K/KN pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. Does not need to be placed on DQS/DQSn pins, but must use a differential pin pair. | Verify Guidelines have been met or list required actions for compliance. |
| Input clock for output data – C and Cn |  | Intel QDRII SRAM interface is implemented in a single clock mode. Connect C and Cn high.  Also look for the connection guidance in the memory device datasheet. | Verify Guidelines have been met or list required actions for compliance. |
| QVLD |  | Intel QDRII+ and QDRII+ Xtreme SRAM interface does not use the QVLD signal. Leave it unconnected on your board. | Verify Guidelines have been met or list required actions for compliance. |
| clock\_source |  | Place it on the PLL reference clock pin as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  Intel does not check these but here are important recommendations for the clock source:  1) Use one of the recommended frequencies shown in the IP (IP General tab -> Clocks),  2) Use a low jitter clock source. See the recommendations for Memory Output Clock Jitter in the [Intel Stratix 10 Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html). | Verify Guidelines have been met or list required actions for compliance. |
| BWSn |  | Place it on BWSN pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Address [A] |  | Place it on address pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Command  [RPS\_N, WPS\_N] |  | Place it on command pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for controller |  | Any user IO pins. The reset pin can alternatively be generated internally. | Verify Guidelines have been met or list required actions for compliance. |
| DOFF\_N |  | Place it on DOFF\_N pin as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ |  | Used when calibrated OCT for the memory interface pins is implemented.  Place it on RZQ pin as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |

**Additional Comments:**

Table 8‑13. Part H: QDRII/II+/II+ Xtreme Termination Guidelines

| Part H: QDRII/II+/II+ Xtreme Termination Guidelines | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Write Clock (K/Kn) @ FPGA |  | Default is HSTL Class I and series OCT 50 Ω with calibration.  You can change output mode to current strength or no termination during IP generation.  Check the termination value in the .qip file  which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Write Clock (K/Kn) @ Memory |  | Write clock at the memory side should be terminated with class I Parallel termination at the memory side. | Verify Guidelines have been met or list required actions for compliance. |
| Read Clock (CQ/CQn) @ FPGA |  | Default is HSTL Class I and parallel OCT 50 Ω with calibration.  You can change input mode to no termination during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Read Clock (CQ/CQn) @ Memory |  | Read clock output impedance is implemented with the help of ZQ input pin on the memory device side. If not, you need to put 50 Ω series OCT on the memory side. | Verify Guidelines have been met or list required actions for compliance. |
| Write data - D @ FPGA |  | Default is HSTL Class I and series OCT 50 Ω with calibration.  You can change output mode to current strength or no termination during IP generation.  Check the termination value in the .qip file  which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Write data – D @ Memory |  | Write data at the memory side should be terminated with class I Parallel termination at the memory side. | Verify Guidelines have been met or list required actions for compliance. |
| Read data - Q @ FPGA |  | Default is HSTL Class I and parallel OCT 50 Ω with calibration.  You can change input mode to no termination during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Read data - Q @ Memory |  | Read data output impedance is implemented with the help of ZQ input pin on the memory device side. If not, you need to put 50 Ω series OCT on the memory side. | Verify Guidelines have been met or list required actions for compliance. |
| BWSn @ FPGA |  | Default is HSTL Class I and series OCT 50 Ω with calibration.  You can also change output mode to current strength or no termination during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| BWSn @ Memory |  | BWSn at the memory side should be terminated with class I Parallel termination at the memory side. | Verify Guidelines have been met or list required actions for compliance. |
| QVLD @ FPGA |  | Intel QDRII+ and QDRII+ Xtreme SRAM interface does not use the QVLD signal. Leave it unconnected on your board. | Verify Guidelines have been met or list required actions for compliance. |
| Address [A] @ FPGA |  | Default is HSTL Class I and series OCT 50 Ω with calibration.  You can also change output mode to current strength or no termination during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Address [A] @ Memory |  | On the memory side, Intel recommends the use of external parallel termination on input signals to the memory. | Verify Guidelines have been met or list required actions for compliance. |
| Command[WPS\_N, RPS\_N]@ FPGA |  | Default is HSTL Class I and series OCT 50 Ω with calibration.  You can also change output mode to current strength or no termination during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Command[WPS\_N, RPS\_N]@ Memory |  | On the memory side, Intel recommends the use of external parallel termination on input signals to the memory. | Verify Guidelines have been met or list required actions for compliance. |
| DOFF\_N@Memory |  | On the memory side, pull-down to GND via 10 KΩ resistor. | Verify Guidelines have been met or list required actions for compliance. |

Table 8‑14. Miscellaneous

|  |  |  |  |
| --- | --- | --- | --- |
| Miscellaneous | | | |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Vref |  | Use a voltage regulator to generate this voltage. | Verify Guidelines have been met or list required actions for compliance. |
| Vtt |  | Use a voltage regulator to generate this voltage. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ |  | RZQ pin is connected to GND through an external 240-Ω or 100-Ω ±1% resistor. Refer to the [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/programmable/documentation/sam1438349166154.html) for the OCT impedance options for the desired OCT scheme. | Verify Guidelines have been met or list required actions for compliance. |

1. The termination schemes suggested in the table are general guidelines. Perform board level simulation for your particular system/board to determine optimal termination scheme.

Table 8‑15. Part I: QDRIV Interface Pins

| Part I: QDRIV Interface Pins | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Data pin – DQA,DQB |  | Place it on DQ pins of the DQ/DQS group. The order of the DQ bits within a designated DQ group/bus is not important. Place the DQA/DQB pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Data inversion pin – DINVA, DINVB |  | Place it on the DQ pins of the DQ/DQS pin group. Place the DINVA/DINVB pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  If the “Data bus inversion” feature is turned off in Intel IP, connect it to GND on your board. | Verify Guidelines have been met or list required actions for compliance. |
| QVLD |  | Place on a DQ pin in the same bank as the read data. Intel IP does not use the QVLD pin. Leave this pin unconnected on your board. You may not be able to fit these pins in a DQS group. | Verify Guidelines have been met or list required actions for compliance. |
| Read clock to the FPGA – QKA/QKAn, QKB/QKBn |  | Place on the corresponding DQS and DQSn pins of the DQ/DQS group.  The polarity of QKB/QKBn must be swapped. QKB pin on FPGA side must be placed on DQSn pin, and QKBn on memory side must be placed on DQS pin.  Please use the <variation\_name>\_readme.txt file which is generated with your IP as a guideline. | Verify Guidelines have been met or list required actions for compliance. |
| Write clock from the FPGA – DKA/DKAn, DKB/DKBn |  | Place DK pins in the same IO bank as the read clock (QK) pins & DQ pins in that byte lane. Please use the <variation\_name>\_readme.txt file which is generated with your IP as a guideline.  DK/DK# must use differential output-capable pins. | Verify Guidelines have been met or list required actions for compliance. |
| Memory clock – CK/CKn |  | Place it on CK/CKn pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| clock\_source |  | Intel does not check these but listedbelow are important recommendations for the clock source:  1) Use one of the recommended frequencies shown in the IP (IP General tab -> Clocks),  2) Use a low jitter clock source. Refer to the recommendations for Memory Output Clock Jitter in the [Intel Stratix 10 Datasheet](https://www.intel.com/content/www/us/en/docs/programmable/683181/current/device-datasheet.html). | Verify Guidelines have been met or list required actions for compliance. |
| Address –  A |  | Place it on A pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Address inversion pin – AINV |  | Place it on AINV pin as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  If the “Address bus inversion” feature is turned off in Intel IP, connect it to GND on your board. | Verify Guidelines have been met or list required actions for compliance. |
| Address parity input –  AP |  | Place it on AP pin as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  If the “Use address parity bit” feature is turned off in Intel IP, connect it to GND on your board. | Verify Guidelines have been met or list required actions for compliance. |
| Address parity error flag – PE# |  | Place it on PE\_N pin as specified in the <variation\_name>\_readme.txt file which is generated with your IP.  If the “Use address parity bit” feature is turned off in Intel IP, you may leave this pin unconnected on your board. | Verify Guidelines have been met or list required actions for compliance. |
| Command –  LDA#,LDB#, RWA#,RWB#,CFG#,  LBK0#,LBK1# |  | Place it on Command pins as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for QDRIV Memory –  RST# |  | Place the RESET\_N signal as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for QDR IV Controller |  | Any user IO pin. The reset pin can alternatively be generated internally. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ |  | Used when calibrated OCT for the memory interface pins is implemented.  Place it on RZQ pin as specified in the <variation\_name>\_readme.txt file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |

**Additional Comments:**

Table 8‑16. Part J: QDRIV Interface Termination Guidelines

| Part J: QDRIV Interface Termination Guidelines | | | |
| --- | --- | --- | --- |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Write Clock (DKA/DKAn, DKB/DKBn) @ FPGA |  | Default is series OCT 34 Ω with calibration.  You can change output mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Write Clock (DKA/DKAn, DKB/DKBn) @ Memory |  | Use QDRIV ODT. Default is 25% of ZT. You can change it to ODT off or other termination value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| Read Clock (QKA/QKAn, QKB/QKBn) @ FPGA |  | Default is parallel OCT 40 Ω with calibration.  You can change input mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Read Clock (QKA/QKAn, QKB/QKBn) @ Memory |  | Use QDRIV Impedance Control. Default is 25% of ZT. You can change it to other drive value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| Memory clocks(CK/CKn) @ FPGA |  | Default is series OCT 34 Ω with calibration.  You can change output mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Memory clocks(CK/CKn) @ Memory |  | Use QDRIV ODT. Default is 25% of ZT. You can change it to ODT off or other termination value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| Data(DQA,DQB) @ Memory |  | Use QDRIV ODT and Impedance Control. Default is 25% of ZT. You can change it to other value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| Data(DQA,DQB) @ FPGA |  | Use Dynamic OCT which is parallel input termination with calibration and series output termination.  Default is series OCT 34 Ω with calibration and parallel OCT 40 Ω with calibration. You can change output mode/input mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| DINV( DINVA, DINVB)  @ Memory |  | Use QDRIV ODT. Default is 25% of ZT. You can change it to ODT off or other termination value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| DINV( DINVA, DINVB)  @ FPGA |  | Default is series OCT 34 Ω with calibration.  You can change output mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| QVLD @ Memory |  | Intel QDRIV SRAM interface does not use the QVLD signal. You can leave it unconnected on your board. | Verify Guidelines have been met or list required actions for compliance. |
| Address (A) @Memory |  | Use QDRIV ODT. Default is 25% of ZT. You can change it to ODT off or other termination value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| Address (A) @ FPGA |  | Default is series OCT 34 Ω with calibration.  You can change output mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP | Verify Guidelines have been met or list required actions for compliance. |
| AINV@Memory |  | Use QDRIV ODT. Default is 25% of ZT. You can change it to ODT off or other termination value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| AINV@FPGA |  | Default is series OCT 34 Ω with calibration.  You can change output mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| AP@Memory |  | Use QDRIV ODT. Default is 25% of ZT. You can change it to ODT off or other termination value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| AP@FPGA |  | Default is series OCT 34 Ω with calibration.  You can change output mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP.  If the “Use address parity bit” feature is turned off in Intel IP, connect it to GND on your board. | Verify Guidelines have been met or list required actions for compliance. |
| PE#@Memory |  | Use QDRIV Impedance Control. Default is 25% of ZT. You can change it to other drive value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| PE#@FPGA |  | Default is parallel OCT 40 Ω with calibration.  You can change input mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP.  If the “Use address parity bit” feature is turned off in Intel IP, leave it unconnected on your board. | Verify Guidelines have been met or list required actions for compliance. |
| Command (LDA#, LDB#, RWA#,RWB#,CFG#,  LBK0#,LBK1#) @ FPGA |  | Default is series OCT 34 Ω with calibration.  You can change output mode to other termination value during IP generation.  Check the termination value in the .qip file which is generated with your IP. | Verify Guidelines have been met or list required actions for compliance. |
| Command (LDA#, LDB#, RWA#,RWB#,CFG#,  LBK0#,LBK1#) @ Memory |  | Use QDRIV ODT. Default is 25% of ZT. You can change it to ODT off or other termination value during IP generation. | Verify Guidelines have been met or list required actions for compliance. |
| Reset for QDRIV@FPGA |  | Use 1.2 V.  Use a pull-down resistor to GND.  Typical value is 10 kΩ, but you should select a suitable value for your implementation.  Refer to the memory vendor’s QDRIV component data sheet for further information. | Verify Guidelines have been met or list required actions for compliance. |

1. The termination schemes suggested in the table are general guidelines. Perform board level simulation for your particular system/board to determine optimal termination scheme.

Table 8‑17. Miscellaneous

|  |  |  |  |
| --- | --- | --- | --- |
| Miscellaneous | | | |
| Plane/Signal | Schematic Name | Connection Guidelines | Comments / Issues |
| Vref |  | Use a voltage regulator to generate this voltage. | Verify Guidelines have been met or list required actions for compliance. |
| Vtt |  | Use a voltage regulator to generate this voltage. | Verify Guidelines have been met or list required actions for compliance. |
| RZQ |  | RZQ pin is connected to GND through an external 240 Ω±1% resistor. Refer to [Intel Stratix 10 General Purpose I/O User Guide](https://www.intel.com/content/www/us/en/programmable/documentation/sam1438349166154.html) for the OCT impedance options for the desired OCT scheme. | Verify Guidelines have been met or list required actions for compliance. |

**Additional Comments:** Reviewed against the [Errata Sheet for Intel Stratix 10 Devices (PDF)](https://www.intel.com/content/www/us/en/docs/programmable/683376/current/gx-device-errata.html) version.

# Document Revision History

|  |  |  |
| --- | --- | --- |
| Date | Version | Changes |
| Feb.2022 | V5.2 | Based on the (PCG-01020-20220114)  (PCG-01020-20211213) |
|  |  | Updated the pin description and connection guidelines of the NAND\_RB pin  Updated the pin description of the nSTATUS pin.  Updated the connection guidelines of the following pins to provide more clarity:  REFCLK\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]p  REFCLK\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]n  REFCLK\_GXP[L, R][10, 11, 12][A, B, C]\_CH[0, 2][p,n]  Updated the connection guidelines of the VCCH\_GXP[L, R][1, 2, 3] pins |
| Jan.2021 | V5.1 | Based on the (PCG-01020-20201223)  (PCG-01020-20201214)  (PCG-01020-20201123)  (PCG-01020-20201023) |
|  |  | Added the RREF\_SIPAUX0 pin in Table: H-Tile and L-Tile Pins  Updated Table: HPS Supply Pins. |
| Aug.2020 | V5.0 | Based on the (PCG-01020-20200807)  (PCG-01020-20200630) |
|  |  | Added Intel Stratix 10 GX 10M pins.  Updated the pin description of the IO3V[0,1,2,3,4,5,6,7]\_[10,12,20,22] pins  Updated the connection guidelines of the GXE(L8, R9)(A, B, C)\_RX\_CH[0:23][p,n] pins  Updated the pin description and connection guidelines of the REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8][p,n] pins  Updated the connection guidelines of the NC pin  Updated the connection guidelines of the U[10, 11, 12, 20, 21, 22]\_P\_IO\_RESREF\_0 pins  Updated the Group 3 valid assignments for the SPIS1\_MISO and SPIS1\_SS0\_N pins  Updated the connection guidelines of the TCK pin  Updated the pin description of the nSTATUS pin  Updated the connection guidelines of the nCONFIG pin  Updated the AVST x8, x16, and x32 configuration schemes for the Direct to Factory Image signal in SDM IO  Removed the SDMMC\_CFG configuration pin functions and connection guidelines from SDM Pins |
| May. 2020 | V4.1 | Based on the (PCG-01020-20200420) |
|  |  | Added the pin description and connection guidelines of the DIFF\_3[A,D]\_[1:24][p,n] pins  Added the pin description and connection guidelines of the IO33\_[5:0]\_[7:0] pins  Added the input reference clock guideline to the following pins:  CLK\_ESRAM\_[0,1]p  CLK\_ESRAM\_[0,1]n  UIB\_PLL\_REF\_CLK\_[00,01]p  UIB\_PLL\_REF\_CLK\_[00,01]n  REFCLK\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]p  REFCLK\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]n  REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8][p,n]  Updated the connection guidelines of the VSIGP\_[0,1] and VSIGN\_[0,1] pins  Updated the connection guidelines of the PWRMGT\_SCL, PWRMGT\_SDA, and PWRMGT\_ALERT signal pins  Updated the connection guidelines of the REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8][p,n] pins  Updated the connection guidelines of the U[10, 11, 12, 20, 21, 22]\_P\_IO\_RESREF\_0 pins |
| March. 2020 | V3.3 | Based on the (PCG-01020-20191213)  (PCG-01020-20191211) |
|  |  | Updated the connection guidelines of the IO3V[0,1,2,3,4,5,6,7]\_[10,12,20,22] pins.  Updated the connection guidelines of the VCCIO3V pin.  Updated the jitter specification of the UIB\_PLL\_REF\_CLK\_[00,01]p and UIB\_PLL\_REF\_CLK\_[00,01]n pins |
| Oct. 2019 | V3.2 | Based on the (PCG-01020-20190701)  (PCG-01020-20190920) |
|  |  | Updated the connection guidelines for the IO3V[0,1,2,3,4,5,6,7]\_[10,12,20,22] pins  Updated the connection guidelines for the REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8]p and  REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8]n pins  Updated the connection guidelines for the PWRMGT\_SCL, PWRMGT\_ALERT, and PWRMGT\_SDA pin  functions in the SDM\_IO pins  Updated the connection guidelines for the UIB\_PLL\_REF\_CLK\_[00,01]p and UIB\_PLL\_REF\_CLK\_[00,01]n  pins.  Updated the connection guidelines for the SDMMC\_DATA3 pin  Updated the connection guidelines of the GXE(L8, R9)(A, B, C)\_RX\_CH[0:23][p,n] pins  Updated the pin description and connection guidelines of the JTAG\_TCK pin  Removed support for the VREFP\_ADC and VREFN\_ADC pins  Added support for Intel Stratix 10 DX devices.  Added Intel Stratix 10 P-Tile Power Supply Pins section  Added Intel Stratix 10 P-Tile Transceiver Pins section |
| May 2019 | V3.1 | Based on the (PCG-01020-20190131) |
|  |  | Correct Legal note  Updated the connection guidelines for VCCR\_GXB and VCCT\_GXB pins |
|  | V3.0 | Based on the (PCG-01020-20181214) |
| Dec.2018 |  | Added direct factory image pin function to pins below  SDM\_IO0, SDM\_IO10, SDM\_IO11, SDM\_IO12, SDM\_IO13, SDM\_IO14, SDM\_IO15, SDM\_IO16  Added SEU\_ERROR and CvP\_CONFDONE pin functions to pins below  SDM\_IO0, SDM\_IO10, SDM\_IO11, SDM\_IO12, SDM\_IO13, SDM\_IO14, SDM\_IO15, SDM\_IO16  Updated OSC\_CLK\_1 pin description  Updated nCONFIG pin description  Updated nSTATUS pin description  Updated the connection guideline of pins IO3V[0,1,2,3,4,5,6,7]\_[10,12,20,22]  Updated the pin description and connection guideline of the VCCFUSEWR\_SDM pin  Updated the pin description and connection guideline of pins below  VCCR\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  VCCT\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  VCCH\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  REFCLK\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]p  REFCLK\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]n  Updated the pin description for the INIT\_DONE function in SDM\_IO0, SDM\_IO5 and SDM\_IO16  Updated the connedtion guideline of the pins below  VCCRT\_GXE(L2,L3,R1,R2,R3)  VCCRTPLL\_GXE(L2,L3,R1,R2,R3)  Updated the connection guideline of the HPS\_COLD\_nRESET function in pins below  SDM\_IO0, SDM\_IO10, SDM\_IO11, SDM\_IO12, SDM\_IO13, SDM\_IO14, SDM\_IO15, SDM\_IO16  Updated the connection guideline of the CLK\_ESRAM\_[0,1]p and CLK\_ESRAM\_[0,1]n pins  Removed support of the Pulse-width Modulation(PWM) mode |
| Oct.2018 | V2.5 | Modify Part A and C of Section V EMIF interface |
| Sep.2018 | V2.4 | Based on the (PCG-01020-20180816) |
|  |  | Added description that following pins can be used for the HPS  TCK, TMS, TDO, TDI  JTAG\_TCK, JTAG\_TMS, JTAG\_TDO, JTAG\_TDI  Added the HPS\_COLD\_nRESET function to pins below  SDM\_IO0, SDM\_IO10, SDM\_IO11, SDM\_IO12, SDM\_IO13, SDM\_IO14, SDM\_IO15, SDM\_IO16  Added the PWRMGT\_ALERT function to pins below  SDM\_IO0,SDM\_IO12  Updated the connection guideline for nPERST[L,R][0:2] pins  Updated the connection guidelines of the pins below  VCCR\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  VCCT\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  Updated the VCCH\_GXB[L,R] pin name to VCCH\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]  Updated the connection guidelines for pins below  GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_RX\_CH[0:5]p  GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_REFCLK[0:5]p  GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_RX\_CH[0:5]n  GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_REFCLK[0:5]n  Updated the pin description for the pins below  REFCLK\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]p  REFCLK\_GXB[L1,R4][C,D,E,F,G,H,I,J,K,L,M,N]\_CH[B,T]n  Updated the connection guidelines of the VCCIO3V pin.  Updated the connection guidelines for the –V device for the PWRMGT\_SCL, PWRMGT\_SDA, and PWRMGT\_PWM0 pin functions of the SDM\_IO pins  Updated the connection guidelines of the VCCRTPLL\_GXE(L2, L3, R1, R2, R3) pins.  Updated the connection guidelines to leave the unused pins floating of the pins below  GXE(L8, R9)(A,B,C)\_RX\_CH[0:23]p  GXE(L8, R9)(A,B,C)\_RX\_CH[0:23]n  Updated the connection guidelines of following pins  REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8]p  REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8]n  Updated the connection guidelines of the VCCL\_HPS pin.  Removed support of the NAND configuration scheme for SDM\_IO pins |
| Dec.2017 | V2.3 | Based on the (PCG-01020-20171221) |
|  |  | Added the following Intel Stratix 10 TX pins  VCCH\_GXE(L2, L3, R1, R2, R3)  VCCRT\_GXE(L2, L3, R1, R2, R3)  VCCRTPLL\_GXE(L2, L3, R1, R2, R3)  VCCCLK\_GXE(L2, L3, R1, R2, R3)  GXE(L8, R9)(A, B, C)\_RX\_CH[0:23]p  GXE(L8, R9)(A, B, C)\_RX\_CH[0:23]n  GXE(L8, R9)(A, B, C)\_TX\_CH[0:23]p  GXE(L8, R9)(A, B, C)\_TX\_CH[0:23]n  REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8]p  REFCLK\_GXE(L8,R9)(A,B,C)\_CH[0:8]n  IO\_AUX\_RREF(11, 12, 20, 21, 22)  Added the following HPS sections  HPS Oscillator Clock Input Pin  HPS JTAG Pins  HPS GPIO Pins  HPS SDMMC Pins  HPS NAND Pins  HPS USB Pins  HPS EMAC Pins  HPS I2C\_EMAC and MDIO Pins  HPS I2C Pins  HPS SPI Pins  HPS UART Pins  HPS Trace Pins  Updated the following pin names  CLK\_ESRAM\_[0,1]p  CLK\_ESRAM\_[0,1]n  RREF\_ESRAM\_[0,1]  Updated the connection guidelines for the following pins  CLK\_ESRAM\_[0,1]p  CLK\_ESRAM\_[0,1]n  UIB\_PLL\_REF\_CLK\_[00,01]p  UIB\_PLL\_REF\_CLK\_[00,01]n  Updated the connection guidelines for the VREFP\_ADC and VREFN\_ADC pins  Updated the connection guidelines for the TEMPDIODEp[0..6] and TEMPDIODEn[0..6] pins  Updated the connection guidelines for the VCCLSENSE and GNDSENSE pins  Updated the connection guidelines for the OSC\_CLK\_1 pin  Updated the connection guidelines for the VCCR\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] and  VCCT\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] pins  Updated the pin names for the VCCM\_WORD\_(BL,TL) and VCCIO\_UIB\_(BL,TL) pins  Updated the pin decription for all SDM\_IO pins to include the resistor information upon device power up  Updated the pin decription for the INIT\_DONE function in SDM\_IO0, SDM\_IO5, and SDM\_IO16  Updated the pin description of the PWRMGT\_SCL function in the SDM\_IO0 and SDM\_IO14 pins  Updated the pin description of the PWRMGT\_SDA function in the SDM\_IO11, SDM\_IO12, and SDM\_IO16 pins |
| July.2017 | V2.2 | Based on the (PCG-01020-20170714) |
|  | Add the TEMPDIODEp[0..6] and TEMPDIODEn[0..6] pins. |
| June.2017 | V2.1 | Based on the (PCG-01020-20170616) |
|  | Add the INIT\_DONE function to SDM\_IO5 and SDM\_IO16 pins  Update the connection guidelines of the pins below  PLL\_[2][A,B,C,F,G,H,I,J,K,L,M,N]\_FB[0], PLL\_[3][A,B,C,F,G,H,I,J,K,L]\_FB[0]  PLL\_[2][A,B,C,F,G,H,wI,J,K,L,M,N]\_FBp, PLL\_[3][A,B,C,F,G,H,I,J,K,L]\_FBp  PLL\_[2][A,B,C,F,G,H,I,J,K,L,M,N]\_FBn, PLL\_[3][A,B,C,F,G,H,I,J,K,L]\_FBn  PLL\_[2][A,B,C,F,G,H,I,J,K,L,M,N]\_CLKOUT[0:1], PLL\_[3][A,B,C,F,G,H,I,J,K,L]\_CLKOUT[0:1]  PLL\_[2][A,B,C,F,G,H,I,J,K,L,M,N]\_CLKOUT[0:1]p, PLL\_[3][A,B,C,F,G,H,I,J,K,L]\_CLKOUT[0:1]p  PLL\_[2][A,B,C,F,G,H,I,J,K,L,M,N]\_CLKOUT[0:1]n, PLL\_[3][A,B,C,F,G,H,I,J,K,L]\_CLKOUT[0:1]n  Update the pin description and connection guidelines of the OSC\_CLK\_1 pin  Update the pin description of the IO3V[0,1,2,3,4,5,6,7]\_[10,12,20,22] pins  Update the connection guidelines of the pins below  RZQ\_[2] [A,B,C,F,G,H,I,J,K,L,M ,N], RZQ\_[3] [A,B,C,D,E,F,G,H,I,J,K ,L]  Update the connection guidelines of the VCCIO([2][A,B,C,F,L,M,N],[3][A,B,C,I,J,K,L]) pins  Update the pin description of the VCCERAM  Update the connection guidelines of the VCCFUSEWR\_SDM pin  Update the connection guidelines of the pins below  VCCR\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  VCCT\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N]  Update the pin description for the CONF\_DONE function in the SDM\_IO5 pin  Update the connection guidelines for the VCCL\_HPS pin  Remove PowerPlay text from tool name |
| April. 2017 | V2.0 | Based on the (PCG-01020-20170224) |
|  |  | Add the following pins for the MX device variant:  VCCM\_[B,T]  VCCIO\_UIB\_[B,T]  ESRAM\_PLL\_REF\_CLK\_[0,1]p  ESRAM\_PLL\_REF\_CLK\_[0,1]n  UIB\_PLL\_REF\_CLK\_[00,01,10,11]p  UIB\_PLL\_REF\_CLK\_[00,01,10,11]n  ESRAM\_RREF\_[B,T]  UIB\_RREF\_[00,01,10,11]  Update IO3V[0,1,2,3,4,5,6,7]\_[10,12,20,22] pin name  Update the connection guideline for the SDM\_IO13 pin  Update the pin description of the CONF\_DONE function in SDM\_IO5 and SDM\_IO16 pin  Update “Quartus II Prime” to “Quartus Prime”  Add “AN692/AN767” document link into Power section  Add “Stratix 10 Configuration User Guide” document link into Configuration section  Add “AN778: Stratix 10 Transceiver Usage” document link into Transceiver section  Update “Stratix 10 General Purpose I/O User Guide” document link in description of RZQ pin |
|  | V1.4 | Move VREF\_ADC, VSIG guideline to Power Section |
|  | V1.3 | Based on the (PCG-01020-1.4) |
|  | Update the VCCPFUSE\_SDM pin name to VCCFUSEWR\_SDM pin.  Update the connection guidelines for OSC\_CLK\_1 pin.  Update the pin description of the AVST\_DATA[31:0] pins.  Update the pin description of the nPERRST[L,R][0:2] pins.  Update the connection guidelines of VCCBAT pin.  Update the connection guidelines of IO3V[0,1,2,3,4,5,6,7]\_[10,12] pins.  Update the connection guidelines of RREF\_SDM pin.  Update the connection guidelines of RREF\_[T,M,B][L,R] pins.  Update the connection guidelines of VCCL\_HPS pin.  Update the connection guidelines of VCCIO([2][A,B,C,F,L,M,N], [3][A,B,C,I,J,K,L]) pins.  Update the connection guidelines of the VCCIO3V pin.  Update the connection guidelines of VCCR\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] pins.  Update the connection guidelines of VCCT\_GXB[L1,R4] [C,D,E,F,G,H,I,J,K,L,M,N] pins.  Update the connection guidelines of VCCH\_GXB[L,R] pins.  Update the connection guidelines of the SDM\_IO5 MSEL[0] pin function.  Update the connection guidelines of the SDM\_IO7 MSEL[1] pin function.  Update the connection guidelines of the SDM\_IO9 MSEL[2] pin function.  Add a reference to AN583 for the VCCPLLDIG\_HPS pin. |
|  | V1.2 | Update EMIF DDR3/DDR4 part  Update nSTATUS pulling up voltage |
|  | V1.1 | Based on the (PCG-01020-1.3)/(PCG-01019-1.0) |
|  | Update “VCCPLLDIG\_SDM” voltage level  Update “REFCLK\_GXB” connection guideline  Move “RREF\_SDM” out of transceiver portion  Update “VCC”/”VCCP”/”VCCL\_HPS”/”VCCH\_GXB”/”VCCT\_GXB”/”VCCR\_GXB” PDN description  Update “GND” with directly statement  Update “INIT\_DONE” pulling up description  Update “AVST\_DATA” connection guideline  Update “Quartus” to “Quartus II Prime”  Update “GXB\_RX”/“GXB\_TX” to “GXB\_RX\_CH”/ “GXB\_TX\_CH”  Correct “Arria 10” to “Stratix 10”, still waiting for Stratix 10 document link available |
|  | V1.0 | Initial release, based on the Device Family Pin Connection Guidelines version 1.3.(PCG-01020-1.3) |