

This document highlights the benefits of variable-precision digital signal processing (DSP) architecture in Altera’s new Arria® V and Cyclone® V FPGAs. Altera’s variable-precision DSP block allows designers to tailor the precision on a block-by-block basis, thereby saving resources and power while increasing performance.

Introduction

DSP designs use hundreds or thousands of multipliers as basic building blocks to implement filters, fast Fourier transforms (FFTs), and encoders that digitally process signals. Depending on the specific type of filter required, varying precision levels may be required within a design at each stage of FIR filters, FFTs, detection processing, adaptive algorithms, or other functions. In addition, DSP algorithms with varying precision levels often require precision higher than 18 bits. The following sections discuss the benefits of Altera’s variable-precision DSP architecture available in Arria V and Cyclone V devices.

Key DSP Design Trends

The range of DSP precision requirements varies by application, as shown in [Figure 1](#). Video applications use multipliers ranging from 9x9 to 18x18. Wireless and medical applications push precision requirements even further when implementing complex, multi-channel filters that must maintain data precision after each filter stage. Military, test, and high-performance computing also push the performance and precision requirements, sometimes requiring single- and double-precision floating-point calculations for implementing complex matrix operations and signal transforms.

Figure 1. Applications and Precision Range



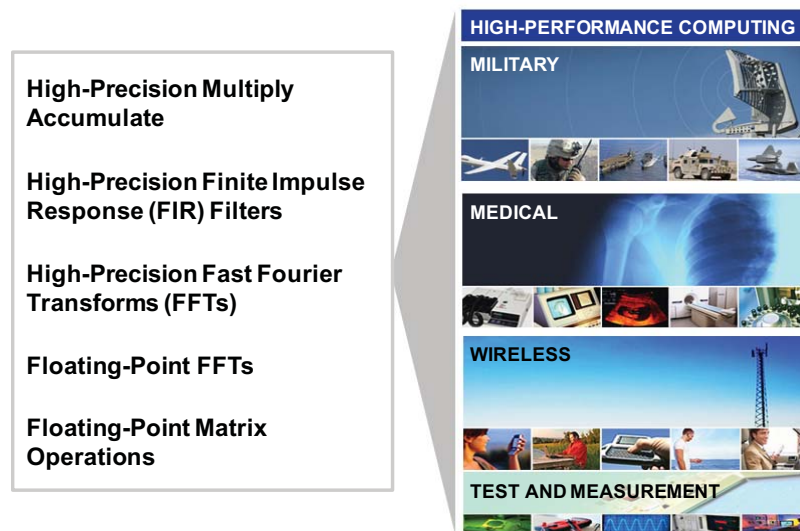
Applications Moving to Variable and Higher Precisions

The DSP architecture of the 28-nm Arria V and Cyclone V FPGAs is optimized to support both high-performance and variable data precision that enables area and power efficient implementation of both fixed and floating-point operations.

High-Precision DSP Applications

Many cutting-edge applications require high-performance DSP designs that support higher than 18-bit precision, as shown in Figure 2. “Precision” in this context means the size of a multiplier, for example 9x9, 12x12, 18x18, 27x27, and other sizes. More specifically, precision refers to the width of each operand applied to a multiplier.

Figure 2. High-Performance Applications



Many traditional DSP functions such as FIR filters, FFTs, and custom signal processing datapaths have high-precision requirements. These functions are commonly implemented in military, medical, and wireless systems. When designs require precision higher than 18-bit, designers may implement floating-point signal processing to reach this precision level in high-end designs, such as military space-time adaptive radars and MIMO processing on LTE channel cards. Altera’s 28-nm silicon architecture introduces the industry’s first variable-precision DSP architecture that allows designers to tailor the precision of each DSP block to perfectly suit the application.

Variable-Precision DSP at 28nm

The variable-precision DSP block in Arria V and Cyclone V FPGAs allow designers to select from 9x9 precision to implement a video processing design, all the way up to floating-point precision required for advanced radar designs. Designers can individually set each DSP block precision to efficiently accommodate bit growth and required precision increases within the DSP datapath. In addition, the Arria V and Cyclone V DSP block is backward-compatible with all modes supported by Altera’s previous generation 65-nm and 40-nm device families. Figure 3 illustrates the precision ranges supported by a single Arria V or Cyclone V DSP block.







Figure 3. Architecture with Selectable Precision



Variable-Precision DSP Blocks

Figure 4 maps the multiplier precision required by various FPGA markets to the supported multiplier precisions in Arria V DSP blocks. The Arria V DSP block natively supports nearly all of precision levels required by these applications. The following sections describe the full-precision, 18x18 with pre-adder mode that is effective in the wireless market.

Figure 4. Precision Requirements and Arria V Precisions

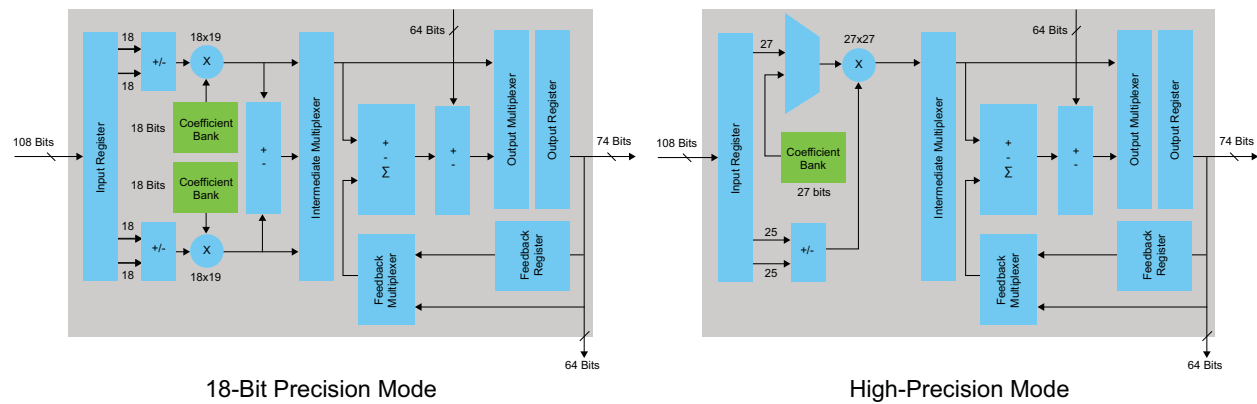
	 Industrial Video	 Broadcast Systems	 Wireless Systems	 Medical Imaging	 Military Radar	 High-Performance Computing
Precision Requirements	9x9	12x12 16x16	18x18	18x18 18x25 18x36 27x27	18x18 18x25 18x36 27x27	27x27 54x54
Arria V Supported Precisions	9x9	12x12 16x16	18x18	18x18 18x25 18x36* 27x27	18x18 18x25 18x36* 27x27	27x27 36x36* 54x54*
Supported Precisions (Competitive FPGAs)	18x25	18x25	18x25	18x25	18x25	18x25

* Requires additional logic outside of the DSP block to implement

Variable-Precision Modes

The Arria V, Cyclone V, and Stratix V DSP block are the first to offer two native precision modes, as shown in Figure 5.

Figure 5. Arria V and Cyclone V DSP Modes



The available modes are 18-bit mode, and high-precision mode for 27x27 multiplications. Figure 6 shows the various multiplier precision modes available in the Arria V (and Cyclone V) DSP block. Designers can implement an 18x36 multiplier by using one DSP block plus additional logic outside the DSP block. Similarly, designers can implement a 36x36 multiplier by using two DSP blocks and additional logic outside the DSP block, or a 54x54 multiplier by using 4 DSP blocks and additional logic outside the DSP block.


Figure 6. Precisions Available in Arria V and Cyclone V FPGAs

Within 1 DSP Block		Within 2 DSP Blocks	
Quantity	Multiplier Mode	Quantity	Multiplier Mode
3	9x9	1	18x18 complex multiply
2	12x12	1	36x36* complex multiply
2	16x16	Within 4 DSP Blocks	
2	18x19	1	18x25* complex multiply
1	18x25	1	18x36* complex multiply
1	27x27	1	27x27 complex multiply
1	18x36*	1	54x54* complex multiply

* Requires additional logic outside of the DSP block to implement

Variable-Precision Efficiency

While the key advantage of variable precision is the ability to take advantage of block-by-block implementation efficiencies, the Arria V variable-precision DSP block also provides the highest number of multipliers of different precisions compared to competing architectures, as shown in Figure 7.

Figure 7. Multiplier Precision Comparison



Multiplier Precision	Arria V & Cyclone V Variable-Precision DSP Block	18x25 DSP48 Block
9x9 (industrial video)	3 per block	1 per block
12x12 (broadcast)	2 per block	1 per block
16x16 (broadcast, digital cinema)	2 per block	1 per block
18x18 (wireless, medical, military)	2 per block	1 per block
18x25 (wireless, medical, military)	1 per block	1 per block
18x36 (medical, military)	1 per block*	0.5 per block
27x27 (military, high-performance computing)	1 per block	0.5 per block

* Requires additional logic outside of the DSP block to implement

2X to 3X Number of Multipliers per Variable-Precision DSP Block Means Power Reduction

DSP Multiplier Comparison

Variable-precision DSP blocks provide significant advantages when implementing multipliers of varying precision. [Figure 8](#) compares an Arria V device of 363 KLEs and 1045 variable-precision DSP blocks, against a Kintex-7 device of 356 KLCs and 1440 DSP blocks. When compared with the Kintex-7 XC7K355T device, the Arria V 5AGXB3 device variable-precision DSP blocks provide a clear advantage when implementing multipliers of different precisions. Nearly across the board, variable-precision DSP blocks provide more multipliers per device.


Figure 8. Arria V FPGA Multiplier Count Comparison


Multiplier Precision	Arria V FPGA 5AGXB3	Kintex-7 XC7K355T
9x9 (industrial video)	3,135	1,440
12x12 (broadcast)	2,090	1,440
16x16 (broadcast, digital cinema)	2,090	1,440
18x18 (wireless, medical, military)	2,090	1,440
18x25 (wireless, medical, military)	1,045	1,440
18x36 (medical, military)	1,045	720
27x27 (military, high-performance computing)	1,045	720

More DSP Resources vs. the Competition

Although competing solutions may offer a few more multipliers in the 18x25 mode, this mode accounts for only a small portion of actual user configurations. [Figure 9](#) provides a comparison of Cyclone V FPGA multipliers against competitive solutions. In general, the Cyclone V device offers more multipliers of different precisions than the Artix-7. The only exception is in the case of 18x25 precision.

Figure 9. Cyclone V FPGA Multiplier Count Comparison



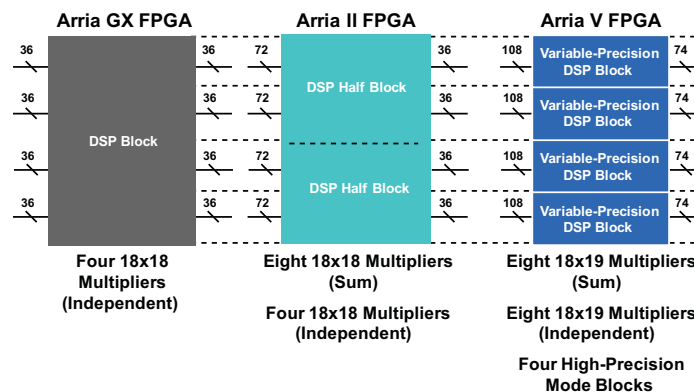
Multiplier Precision	Cyclone V FPGA 5CGXC4	Artix-7 XC7A50T
9x9 (industrial video)	210	120
12x12 (broadcast)	140	120
16x16 (broadcast, digital cinema)	140	120
18x18 (wireless, medical, military)	140	120
18x25 (wireless, medical, military)	70	120
18x36 (medical, military)	70	60
27x27 (military, high-performance computing)	70	60

More DSP Resources vs. the Competition

DSP Block Evolution

Altera’s DSP block architecture has evolved at each process node over time, as illustrated in [Figure 10](#). The fundamental theme of this evolution is backwards-compatibility and new features that support the next generation of DSP system designs.

Figure 10. Evolution of DSP Blocks in Arria V FPGA



Historically, the Arria device DSP block implemented four independent 18x18 multipliers. The Arria II device DSP block continues to support this mode and adds more efficient implementation of eight 18x18 multipliers in “sum” mode via a 44-bit cascade bus. Designers can effectively use this mode to implement common FIR filter structures.

The latest 28-nm, variable-precision DSP blocks in Arria V and Cyclone V devices maintain compatibility with previous generation devices, while increasing capability for higher precision signal processing. The Arria V and Cyclone V DSP block architecture fabric is enhanced to implement the highest performance and highest precision DSP application data paths.

Key DSP Enhancements

Arria V and Cyclone V DSP blocks include the following enhancements:

- Pre-adders
- 18x19 Multipliers
- Coefficient Banks
- Feedback Registers
- Independent Multipliers

The following sections discuss these enhancements in greater detail.

Pre-adders

The Arria V and Cyclone V DSP block is enhanced to include pre-adders to reduce multiplier count in symmetric FIR filters, as shown in Figure 11. These pre-adders accept full 18-bit operands, including sign bits. These pre-adders are referred to as “hard” pre-adders because they are implemented in dedicated hardware resources, rather than as FPGA logic gates.

Figure 11. Pre-Adders High Level View

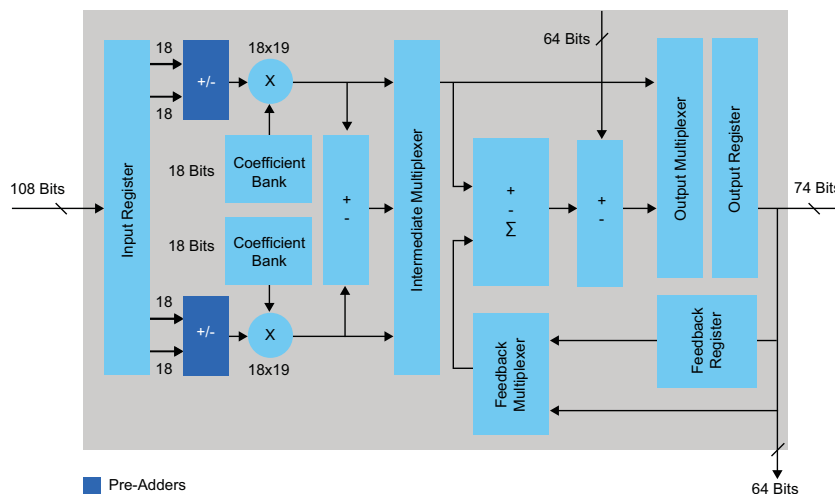


Figure 12 provides a more detailed view of the hard pre-adders. The next section provides an example application that uses pre-adders in a FIR filter design.

Figure 12. Hard Pre-Adder Detail

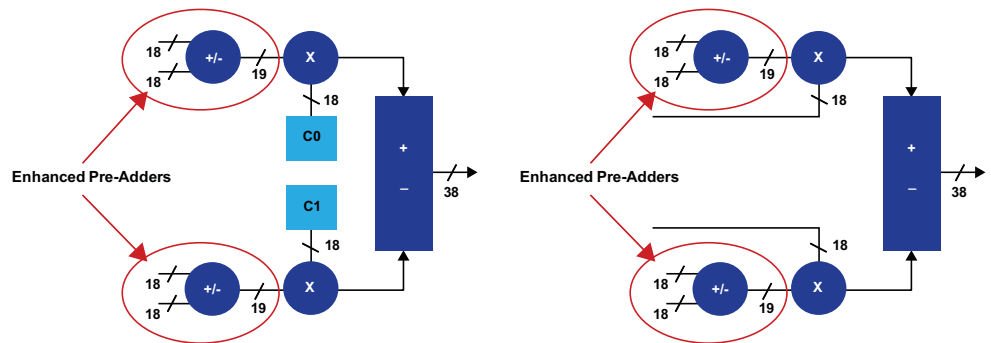
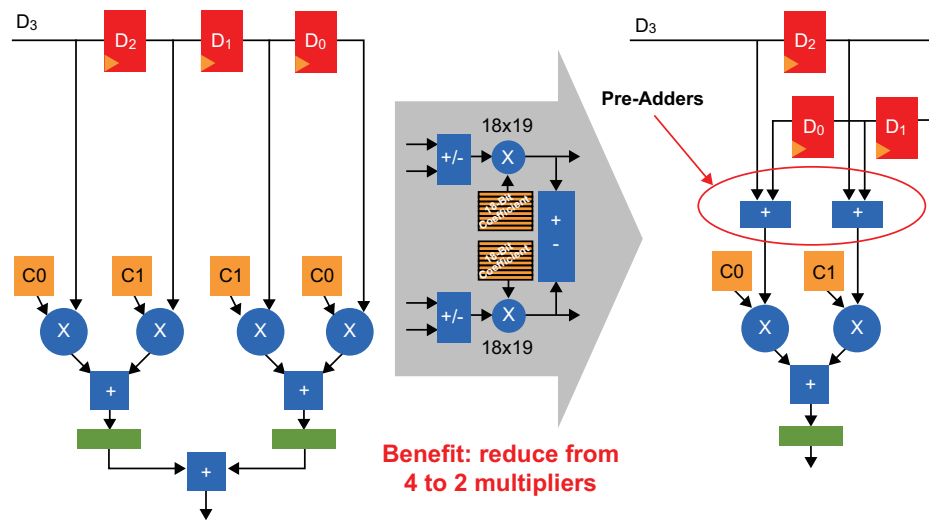


Figure 13 illustrates the use of pre-adders in a FIR filter. Typically designers use pre-adders for building symmetric FIR filters. As the filter data is shifted across the coefficient set, two data samples can be multiplied by a common coefficient due to the symmetry. The pre-adder adds two samples prior to multiplication, which allows the use of one, rather than two, multipliers for every two data samples. Pre-adders reduce by half the number of required multipliers for symmetric FIR filters, and eliminate the need to implement such adders using the logic gates in the FPGA. This technique increases logic efficiency and performance. Designers can use this hard pre-adder as either a dual 18-bit pre-adder, or as a single 27-bit pre-adder, depending on the required precision.

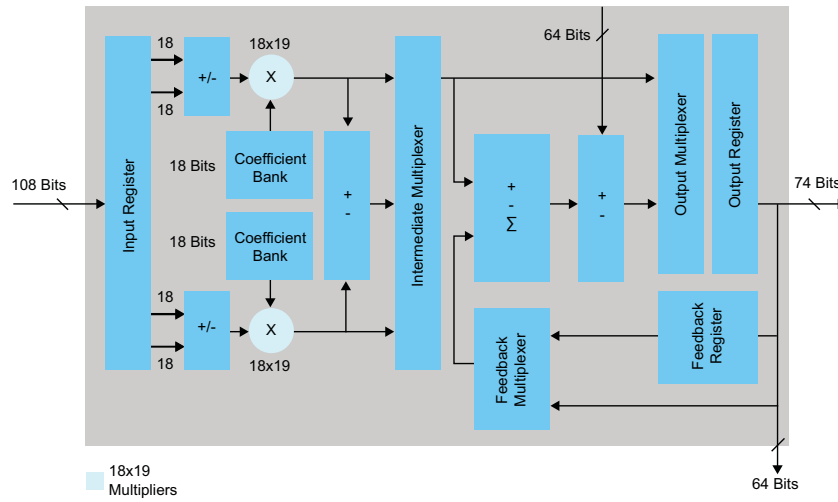
Figure 13. Usage of Pre-adders in Symmetric FIR Filter



18x19 Multipliers

The Arria V and Cyclone V DSP block is enhanced to include an 18x19 multiplier, as shown in Figure 14.

Figure 14. 18x19 Multipliers



Previous generation devices included only an 18x18 multiplier. The 18x19 multiplier accepts 19-bit results from the output of the 18+18 pre-adder. Designers can use the extra bit in each pre-adder operand to represent the + or - sign of each operand. Figure 15 shows a close-up view of the 18x19 multiplier.

Figure 15. Close-up View of 18x19 Multiplier

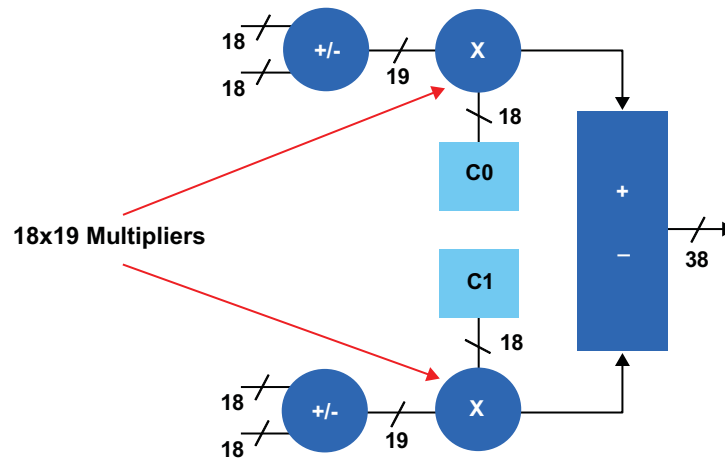
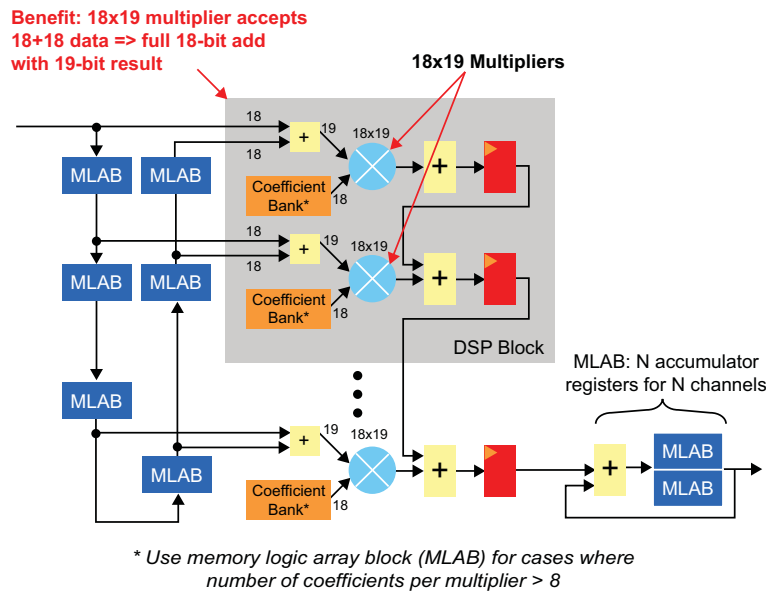


Figure 16 illustrates an example application of the 18x19 multiplier.

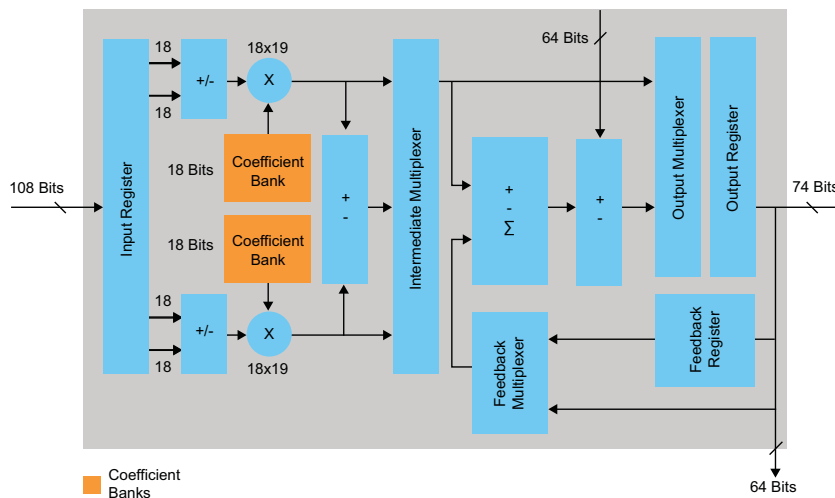
Figure 16. Usage of 18x19 Multiplier



Coefficient Banks

Arria V and Cyclone V DSP blocks include a coefficient storage bank that is dynamically selectable on each clock cycle, as illustrated by Figure 17.

Figure 17. Coefficient Blocks within the DSP Block



This feature is especially helpful in DSP designs that include FIR filters implemented in hardware using a parallel or partially parallel structure, which often require only a small number of coefficients per multiplier. Altera’s variable-precision DSP architecture provides an internal coefficient bank that designers can set to support 18-bit and higher precision signal processing. In 18-bit mode, the coefficient bank is

configured as two, 18-bit wide register banks, each capable of storing eight coefficients per multiplier. In the high-precision mode, the coefficient bank is configured as a single, 27-bit wide register bank capable of storing eight coefficients per multiplier. The coefficient banks allow designers to select which of the eight registers should be used as a coefficient source for the multiplier for every clock cycle.

Use of the internal coefficient bank eases timing closure complexity and reduces on-chip memory and register resource usage, both of which are critical in DSP designs. Figure 18 shows the coefficient bank in the 18-bit mode and in the 27-bit mode.

Figure 18. Structure of Coefficient Bank

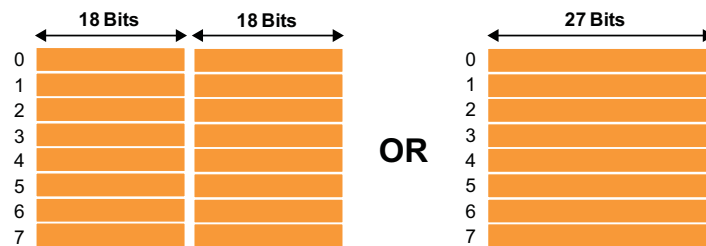
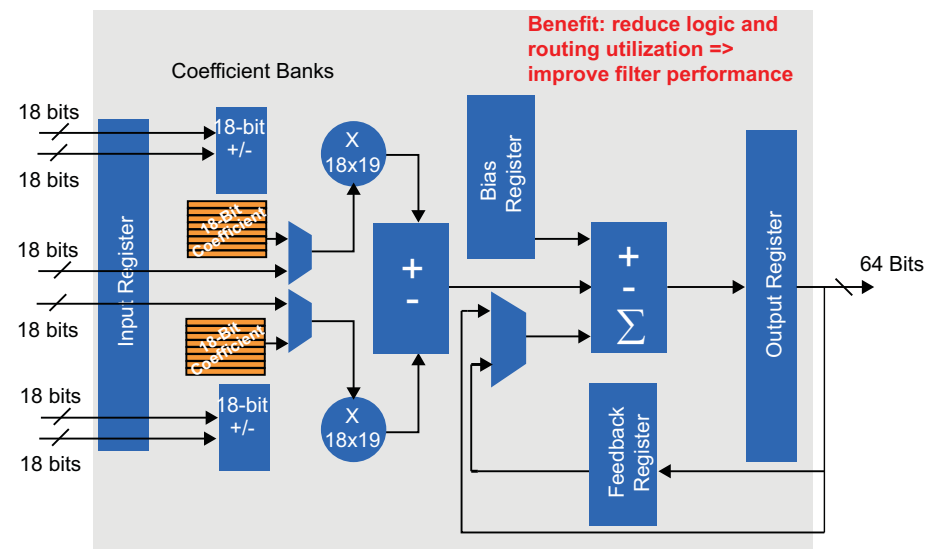


Figure 19 shows how a serial filter is implemented, making use of the two 18-bit coefficient banks. The DSP architecture of the Arria V and Cyclone V FPGA effectively supports this type of filter because the coefficient banks, the 18x19 multipliers, and the output register are all contained in one DSP block. In addition, the output can be cascaded to the next block in a sequential chain. Having the coefficient bank inside the DSP block reduces logic and routing utilization, thus improving filter performance.

Figure 19. Usage of Coefficient Bank in Filter



Feedback Registers

Arria V and Cyclone V DSP blocks include feedback registers that can serve as the second stage in a two-stage accumulator comprised of the output register and feedback registers. The relative position of the feedback register in the DSP block is illustrated in Figure 20.

Figure 20. Feedback Register

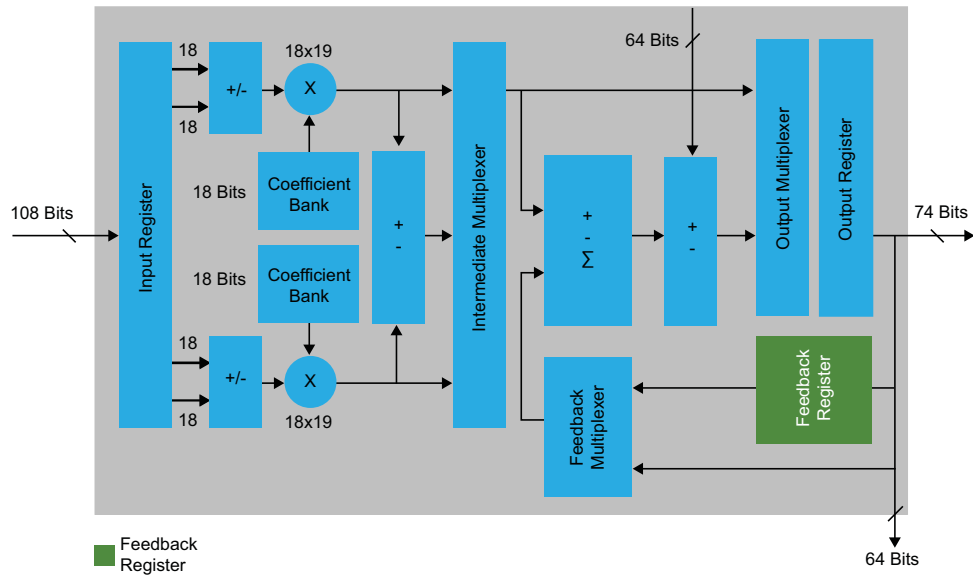
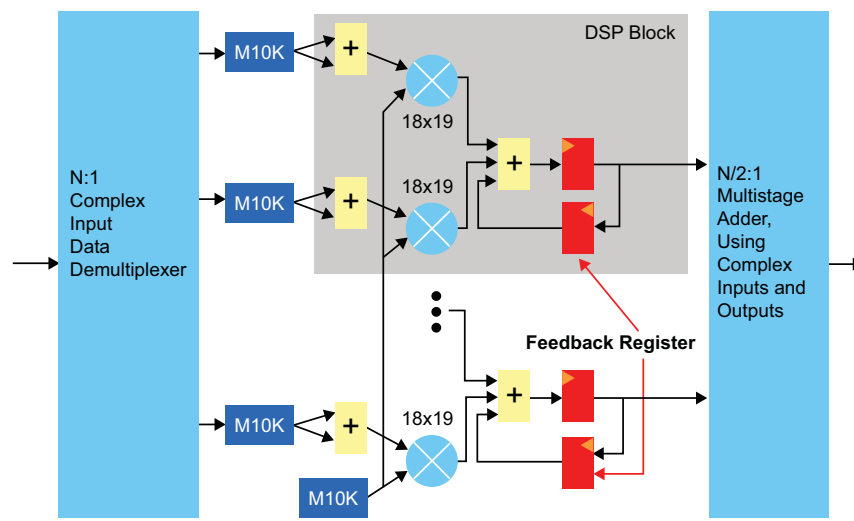


Figure 21 shows how a polyphase serial filter is implemented, with the feedback register enabled to provide a feedback path. This structure enables two independent serial-filter channels in one single DSP block. Each channel has its own set of input. The feedback path is time multiplexed, allowing processing of the real part and the imaginary part of a complex signal in alternating clock cycles. Only $N/2$ adders are needed because the Arria V and Cyclone V DSP block in 18-bit mode has two 18x19 multipliers per DSP block. This implementation is efficient and saves resources.

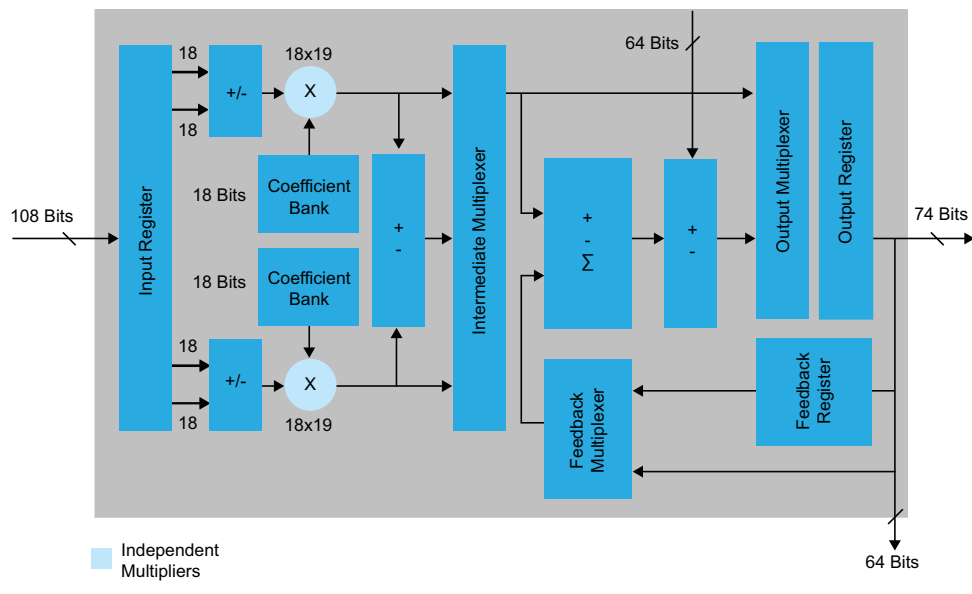
Figure 21. Feedback Register Usage



Independent Multipliers

Arria V and Cyclone V DSP blocks include independent multipliers. This means that the output(s) of the multiplier(s) can be routed to the output port of the DSP block directly, without going through any adder. Figure 22 shows two 18x19 multipliers which can be configured to work in the sum mode or independent mode

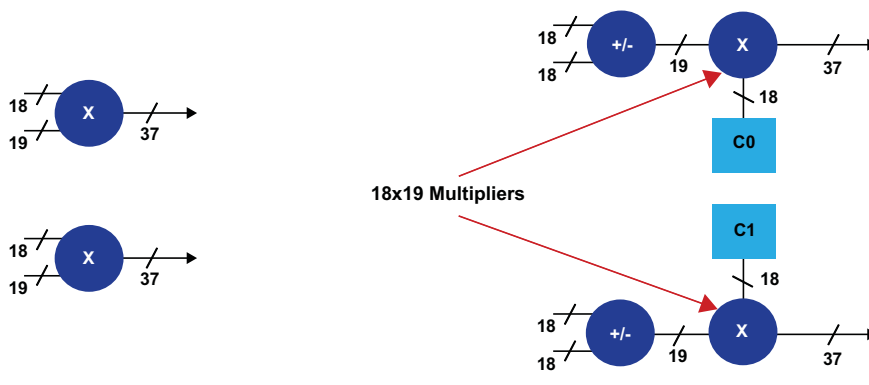
Figure 22. Input/Output Ports



Each DSP Block contains two 18x19 multipliers. These blocks can be used as two completely independent multipliers with inputs fed from outside the DSP block, as shown on the left-hand side of Figure 23, or each multiplier having one operand fed from a coefficient bank, and the outputs of the multipliers delivered independently, as shown on the right hand side of Figure 23.

The output port of the DSP block in Arria V and Cyclone V is 74-bits wide and therefore can accommodate the output of 37 bits of the two independent 18x19 multipliers. This means that all 37 bits from each multiplier are directly accessible on the output port.

Figure 23. Application Example



Altera Floating-Point Precision

Depending on the application, the precision requirement may require that multiplications are performed with single-precision, floating-point multiplications, or double-precision, floating-point multiplications. The Arria V and Cyclone V DSP block is capable of both levels of precision, as described in the following sections.

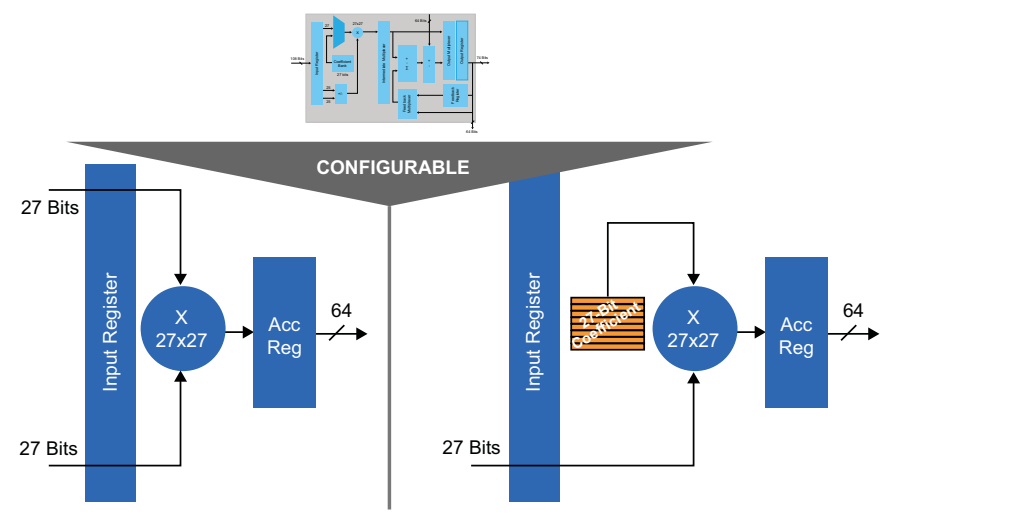
IEEE Standard 754 floating point is the most common representation of floating-point numbers. In this format, single-precision floating point is 32-bits wide with a 24-bit mantissa, while double-precision floating point is 64-bits wide and has a 53-bit mantissa.

Floating-point computations involve mantissa multiplication and exponent addition. The Altera variable-precision DSP architecture can implement mantissa multiplication for a single-precision, floating-point number using one block OR mantissa multiplication for a double-precision, floating-point number.

Single-Precision Floating-Point Multiplication

Using the high-precision mode, the variable-precision block is uniquely suited for implementing single-precision, floating-point operations. Mantissa multiplication can be implemented using only one variable-precision block configured in the high-precision mode. This resource efficiency is an FPGA industry first. Traditionally designers had to cascade multiple blocks to implement this operation. The coefficients may be applied externally as shown on the left-hand side or internally as shown on the right-hand side in Figure 24. Competing DSP architectures with 18x25 bit resolution require multiple blocks, as well as external logic to implement a floating-point mantissa multiplication, resulting in a lower performance and higher power implementation.

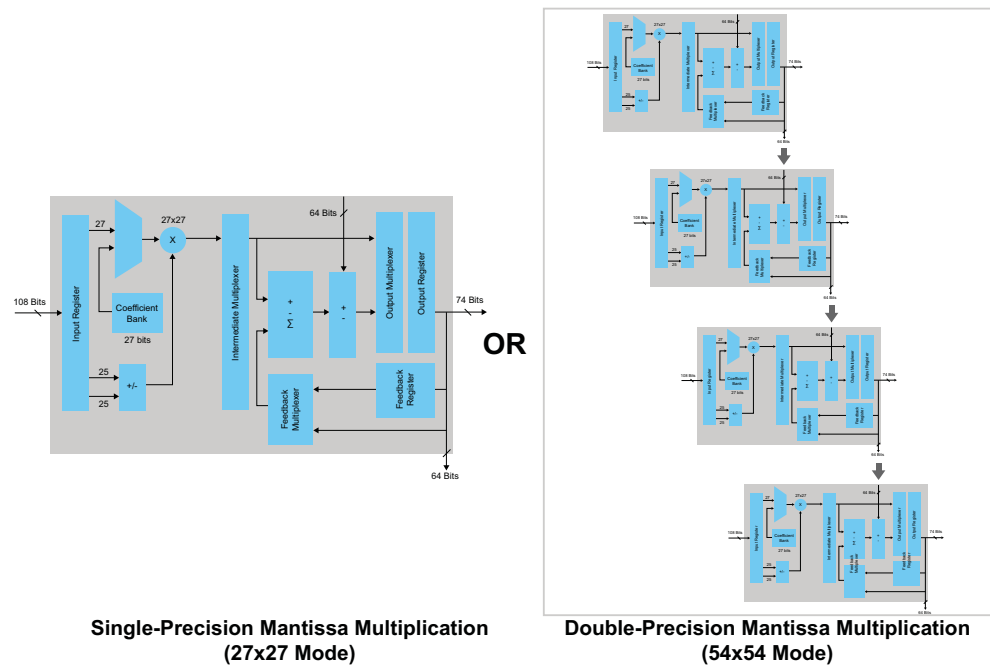
Figure 24. Single-Precision Floating-Point Multiplication



Double-Precision Floating-Point Multiplication

Double-precision mantissa multiplication requires four DSP blocks all cascaded by using the dedicated 64-bit cascade bus in the DSP block, as shown in [Figure 25](#).

Figure 25. Floating-Point Modes



This technique is an FPGA industry first, because competing architectures require cascading two 18x25 blocks for single-precision, floating-point mantissa multiplication and up to nine blocks (with extra logic) to implement a 54x54 double-precision mantissa multiplier.

Competitive Summary

With the introduction of the variable-precision DSP architecture, Altera has opened a DSP technology gap against competing architectures, as summarized in [Figure 26](#). Altera's latest 28-nm devices can natively, and within a single block, implement a 27x27 multiplier useful for high-precision, fixed-point DSP, or for emerging floating-point DSP applications. Variable precision means that designers set the DSP architecture precision to match the algorithm, not the other way around. Also with a 64-bit cascade bus and accumulator, designers don't have to forgo precision when the algorithm implementation requires multiple DSP blocks.

Figure 26. Competitive Comparison

Feature	Xilinx	Arria V and Cyclone V FPGAs
Native support for 27x27 multiply mode		✓
Variable-precision multiplier size: 27x27 or 18x19 (dual)		✓
Efficient implementation of floating point		✓
Coefficient register banks within the DSP block		✓
Efficient 2-stage accumulator (feedback register)		✓
Accumulator size	48 bits	64 bits
Width of cascade bus	48 bits	64 bits
Pre-adder support for symmetric filters	✓	✓
Support for systolic FIR filters	✓	✓

Conclusion

Altera's variable-precision DSP block allows the designer to tailor the precision on a block-by-block basis. For symmetric filters, hard pre-adders in the DSP block reduce the required multiplier count by 50%, thus saving resources and power. The 18x19 multipliers accommodate full 18+18 addition, including sign bits. Internal coefficient banks enable higher multiplier performance and save logic resources.

The Arria V and Cyclone V DSP block is optimized for FIR filters, and the feedback register allows implementation of two independent serial-filter channels per DSP block. The independent multipliers allow operands to be applied directly to the multipliers and allow the multiplier outputs to be observed directly on the DSP block output port. Finally, Altera offers the industry's first floating-point function in an FPGA architecture.

Further Information

- Arria V FPGA Family Overview
<http://www.altera.com/products/devices/arria-fpgas/arria-v/overview/arrv-overview.html>
- Arria V Device Family Advance Information Brief
http://www.altera.com/literature/hb/arria-v/av_51001.pdf
- Cyclone V FPGA Family Overview
<http://www.altera.com/products/devices/cyclone-v-fpgas/overview/cyv-overview.html>
- Cyclone V Device Family Advance Information Brief
http://www.altera.com/literature/hb/cyclone-v/cyv_51001.pdf

Acknowledgements

- Pat Fasang, Senior Member of Technical Staff, DSP Marketing, Altera Corporation