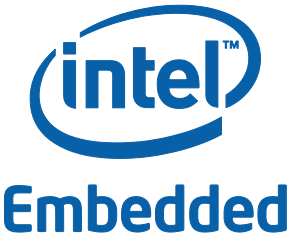

White Paper

Sathish Venkataramani
Technical Marketing Engineer
Intel Corporation

Advanced Board Bring Up - Power Sequencing Guide for Embedded Intel Architecture

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Executive Summary

Board Debug is a critical component in the design path of Embedded IA boards. The topic is very broad and pertains to a lot of functional areas on the platform. This paper concentrates in the area of power sequencing and the debug involved on Embedded IA platforms.

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Tables and Figures

Introduction

Intel® Architecture designs in embedded systems have been present for a long time, however the complexity of the systems have grown almost exponentially with each generation of the IA architecture adding more hardware features and more devices to the system. This addition of devices means the power supply into the board needs to be robust to support the various devices. Apart from the power supply being robust the entire power subsystem and routing on the board including the sequencing needs to be spot on so that the board can power up without any issues.

In my previous whitepapers, I have given the basics of what to look for on the board before you power on the system and also how to check the accuracy of the layout of the board. There was also a brief introduction to general power sequencing. The objective of this paper is to take the board bring up a step further and show the process from actual power on to the point where you start fetching code from the BIOS. We will have a detailed look at the Embedded IA board with respect to the signals that make up the majority of the power up sequencing and how the entire circuitry can be deciphered easily.

Terminology

Term	Description
ICH	I/O Controller Hub
PCH	Platform Controller Hub
IOH	I/O Hub
POST	Power On Self Test

Reference

Reference	Document Number
High Speed Digital Design Principles	321091
Embedded Intel® Architecture Board Bring Up Procedure	322504
Text editor software	Ultra Edit - http://www.ultraedit.com/ Notepad(freeware) - http://notepad-plus-plus.org/
Calpella Platform Power Sequencing Specification	393353
Wikipedia Page for BIOS/EFI	www.wikipedia.com

Before Power on - Tools of the Trade

Embedded Intel® Architecture boards follow similar guidelines to the mobile and desktop platforms based on the performance needs of the design. These guidelines are normally published as embedded collateral at the Embedded Design Center. If a customer is designing the board to launch along with Intel they will need NDA access to get the documents through Intel Business Link or IBL. The main documents needed for a board design are the following.

1. Platform Design Guide
2. Processor Power Delivery Guideline
3. IA System BIOS writers guide for the specific processor
4. Design files of Intel Reference board (schematics and board files)

One of the greatest tools for a board engineer would be the free PCB/board file viewer. There are a lot of vendors available such as Cadence, Mentor and Altium (formerly Protel) that offer good free viewers of the board files of the design. It is imperative that this tool be available in the lab where board bring up is planned. It is always good to have a background in soldering wire for quick fixes or at least have a technician to help out when soldering is required.

You will also need the following lab tools:

1. Oscilloscope – Very important for tracking signals and also the timing
2. Debug Port 80 cards (For designs that do not have onboard debug LEDs)
3. ITP (In Circuit Target Probe)
4. Software testing tools (once the board is booting)

There is a lot of material available on oscilloscopes online as well as from the vendors themselves. Let us look as the second item listed above.

The debug port 80 card has been used in Intel designs for a long time and is a great tool to have when you are debugging BIOS halts and early bring up cycles of the processor.

Note: Many newer board designs have this as a part of the board.

The LED panel is present a surface mount part. This device plugs onto the LPC bus header on the board. The LEDs flash codes during boot up sequence and the series of codes are various checkpoints during the bios boot up

sequence. It is very important to know what the codes stand for as they will call out in detail the exact point of failure. If a halt should occur at a certain code, the engineer can then single step through to figure out where the problem is or try to work around it by completely bypassing that piece of code untill it gets fixed.

The Intel ITP or Intel in Target Probe is one of the most important tools for a bios/hardware engineer debugging issues that relate to the processor and memory. The tool gives access to the various MSRs (model specific registers) which lets the engineer control very specific features of the processor such as memory bus speed or error correction. As a customer of Intel products you have a list of vendors who provide the ITP for testing the platform and processor.

Finally the software tools are of paramount importance. There is a long list of software tools that can be used for bring up. The following tools are definitely high on the priority list before a board bring up.

1. Firmware programmer (BIOS, ME firmware etc)
2. BIOS Debugger utility, essentially a code viewer for debugging the BIOS on the fly during bring up. Check the reference section for a couple of common text editors which are used for viewing and editing code.

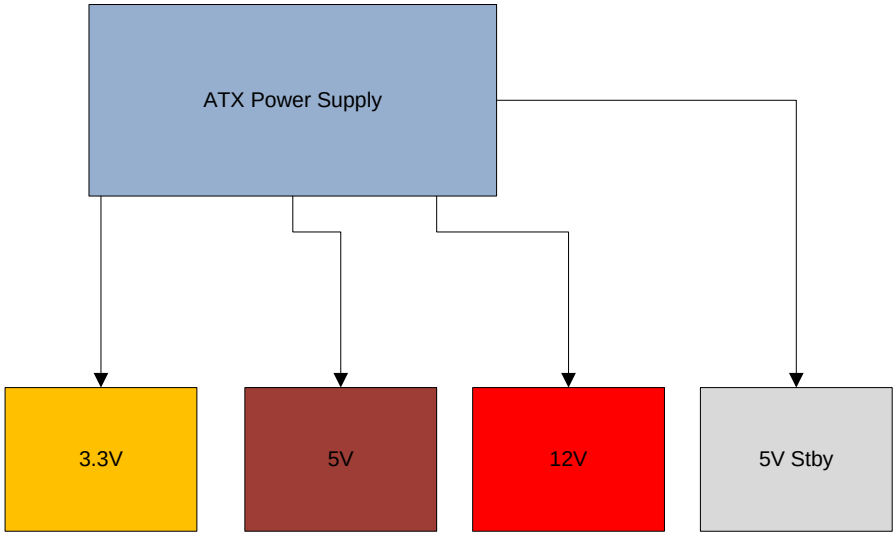
Power On and Sequencing

This section will focus on the various power rails in the system and how power sequencing works on an Intel motherboard.

Note: The information in this document is specific to the Intel® Core™ processor with the Mobile Intel® 5 Series Chipset platform and may be applicable for platforms featuring the 2nd Generation Intel® Core™ processor designs. Please check the chipset version and specification for the right power sequencing information.

The following figure shows the main rails in a system coming from the Power Supply.

Figure 1 General Power System Block diagram



We can see from Figure 1 that the main rails into the system are the 12V, 3.3V, 5V and also a 5V Stby. We will discuss more about the three main rails above, namely the 3.3V, 5V and the 12V. These voltages are used as the inputs on the various regulators on board. These in turn generate lower voltages for use on the board. Table 1 below shows a sample diagram of how many different voltages are required on board for a system without an M3 state.

Table 1 Voltages required by a System with no M3 state

System with No M3 State Supported

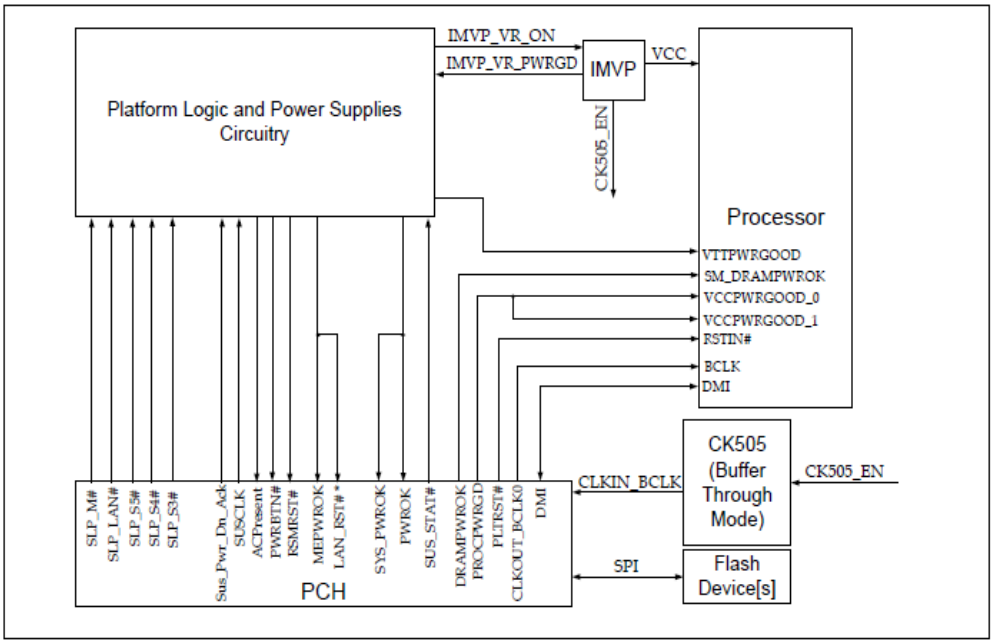
Rails	S0/M0	S3/Moff	S4/Moff	S5/Moff	G3
VBATA (VDC)	ON	ON	ON	ON	No Power
RTC Well	ON	ON (1)	ON (1)	ON (1)	ON
V5.0A	ON	ON	ON	ON	No Power
V3.3A	ON	ON	ON	ON	No Power
V3.3M	ON	OFF (2)	OFF (2)	OFF (2)	No Power
V1.1M	ON	OFF	OFF	OFF	No Power
V1.5U(VDDQ)	ON	ON	OFF	OFF	No Power
V0.75S	ON	OFF	OFF	OFF	No Power
V5.0S	ON	OFF	OFF	OFF	No Power
V3.3S	ON	OFF	OFF	OFF	No Power
V1.8S	ON	OFF	OFF	OFF	No Power
V1.5S	ON	OFF	OFF	OFF	No Power
V1.1S	ON	OFF	OFF	OFF	No Power
V1.1S_VTT	ON	OFF	OFF	OFF	No Power
VccGfx	ON	OFF	OFF	OFF	No Power
Vcore	ON	OFF	OFF	OFF	No Power

From the list above, the amount of voltages that make up the power system on the board is a considerable number. To ensure that all of the above voltages are in spec, the engineer is advised to work with the VR (voltage regulator) vendors.

The entire platform power is controlled by the power sequencing logic, which is made up of the discreet logic on board as well as the power sequencing code present on the embedded controller. The control process keeps track of all the signals starting from the power button push to the platform reset signal appearing, which signals the start of the processor fetching code.

Figure 2 2 below shows the platform power block diagram used on platforms based on the Intel® Core i7™ Processor or Intel® Core™ i5 Processor with Mobile Intel® QM57 Express Chipset.

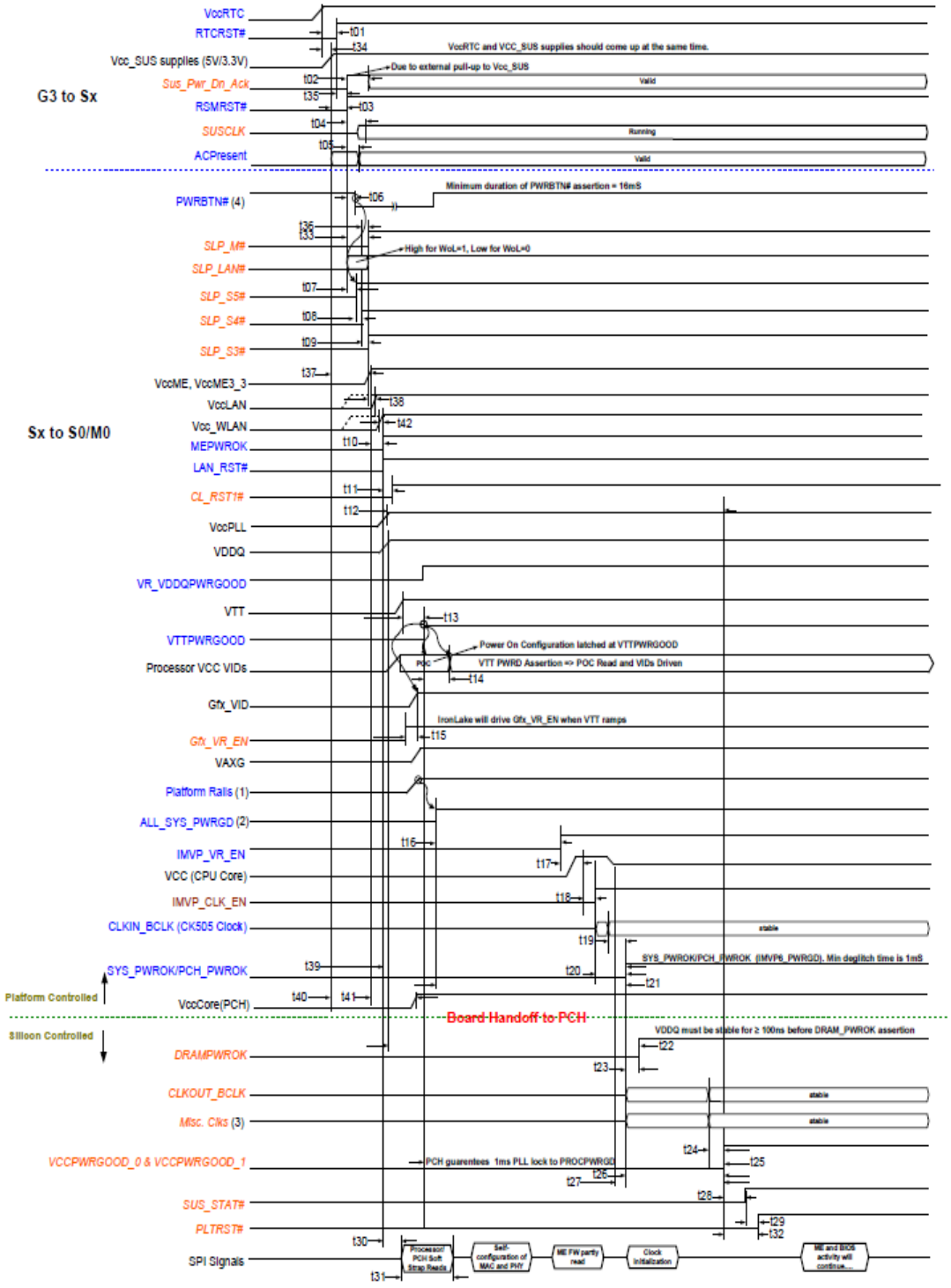
Figure 2 Platform Power Logic and Signal Block Diagram



We can see that the power sequencing is accomplished by the interaction between the Power logic, the Platform controller Hub (Chipset), and the IMVP (Processor voltage regulator). For more information on the signals mentioned in the diagram above please check the Calpella Platform Power Sequence specification document mentioned in the Reference section.

Furthering this discussion, the Figure 3 shows the power on sequence that the platform should follow from a system off condition. The figure shows the major voltages involved and the pattern in which they all should fire in order to get the system to power on. For more information on the individual "T" numbers mentioned in the diagram please refer to the Calpella Platform Power Sequence specification document mentioned in the Reference section.

Figure 3 Power Sequence timing Diagram from S4-5/Moff to S0/M0

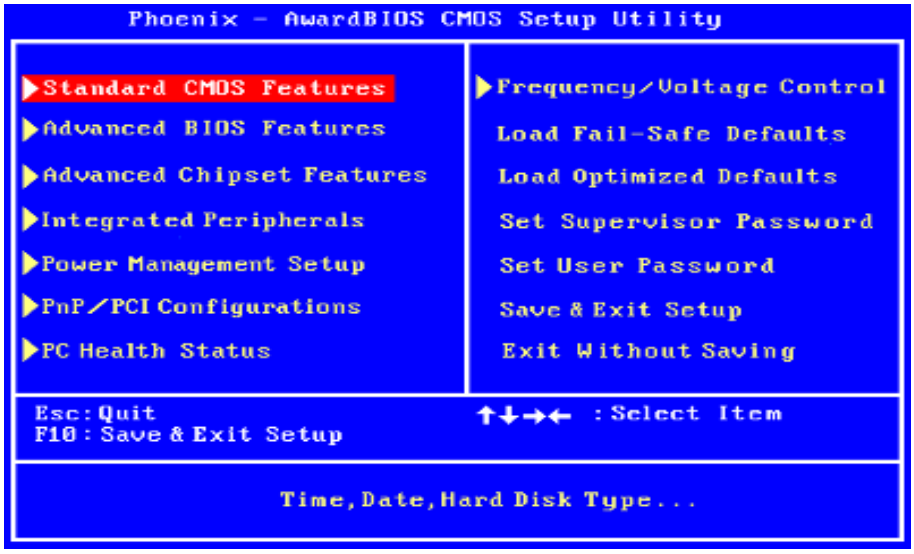


BIOS/EFI

Once the platform reset signal is active and the platform is out of reset, the processor will start the fetching of the BIOS code. BIOS (Basic Input/Output System) is a major factor in the boot up of a platform. Most of the Intel based boards will have BIOS manufactured by an Intel specified BIOS vendor. A board manufacturer can choose to take any of these BIOS and then work with the vendor on further tweaking it. Some board manufacturers write and code their own BIOS for each of their systems with specific features built in to them, such as support for ECC memory[1], support for different speeds of memory, etc. No matter what the case, the BIOS is a code that needs to be worked on meticulously or there is a high probability that the system will fail to run even though all the power and system signals are good.

BIOS needs to load the system and initialize all the devices so that the operating system can start loading. The secondary function of modern BIOS is that it provides a GUI in which a user can configure a system and its devices to operate under different conditions. For example, USB devices can be made to run only at USB 1.1 speeds for debug purposes or the processor bus speed can be targeted to either a higher or lower speed based on user needs. The following figure shows a screen shot of a Phoenix BIOS screen (source: Wikipedia).

Figure 4 A BIOS GUI Screen Shot



[1] Supported only on select platforms.

BIOS, however is currently becoming a legacy method of turning systems on. UEFI or Unified Extensible Firmware Interface is the new method of booting up a system. The original EFI specification was developed by Intel, and that defined the software interface between the operating system and the platform firmware. As stated on the UEFI page of Wikipedia, the newer UEFI firmware provides several advantages over the previous EFI as well as the common BIOS such as:

- Ability to boot from large disks (over 2TB)
- Faster boot-up
- CPU-independent architecture
- CPU-independent drivers
- Flexible pre-OS environment, including networking support
- Modular design

For more information on EFI/UEFI please see the reference sections.

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Authors

Sathish Venkataramani is a Technical Marketing Engineer with Embedded Communications Group at Intel Corporation.

Acronyms

GUI Graphical User Interface

BIOS Basic Input / Output System

EFI Extensible firmware Interface

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